PMOSFET AND NMOSFET
BROADBAND MIXER DESIGN

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We certify that we have read this thesis and that, in our opinion, it is satisfactory in scope and quality as a thesis for the degree of master of science in Electrical Engineering.

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Abstract

In this thesis work, three double balanced resistive mixers realized in a 0.25 \( \mu \)m CMOS TSMC process were designed and fabricated in order to obtain low conversion loss and high input third order intercept point (IIP3), and in order to compare the flicker noise of NMOSFET to PMOSFET. These mixers were designed for wireless applications with RF and IF frequency ranges of 1 to 3 GHz, and DC to 50 MHz, respectively. The mixer design process as well as simulated and measured results are given and discussed. A measured conversion loss of 10.1 dB, 21.8 dB and 14.8 dB of NMOSFET and PMOSFET mixers has been achieved respectively. Measured linearity values are 7 dBm, 17 dBm and 14 dBm for 1dB compression point and 12 dBm, 7 dBm and 19.25 dBm for third order intercept point. All measured isolation values are higher than 45 dB between all ports. The circuit was simulated using Agilent ADS software with BSIM3v3 transistor models and the layout has been carried out in Cadence. These mixers achieve a broadband performance, at moderate conversion loss.
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Chapter 1

1. Introduction

1.1. Motivation

Recent growth of wireless communication systems has motivated the development of high performance, low cost, radio transceivers. One of the key circuits in wireless transceiver modules is the mixer used for up-conversion of modulated data stream on the transmitter side, and for down-conversion to frequencies where analog signals can be readily digitized and further processed on the receiver side. Mixers offering low conversion loss, low intermodulation distortion (IMD) and requiring low LO power play a critical role in the performance of RF front-ends. A mixer produces the intermediate frequency (IF) of sum and difference between radio frequency (RF) and local oscillator (LO). In general, a balanced diode mixer and an active mixer provide the required linearity for the transmission, but those mixers cannot achieve the linearity required for a distortion-less transmission of nonlinear modulated signals. Only a double balanced resistive mixer with high linearity, good port to port isolation due to differential LO signal and low power consumption are superior to diode and active mixers in their intermodulation suppression performance. Therefore, these mixers will play a more important role in future transmitter architecture.
In this thesis work, we examine the double balanced resistive mixer design implemented in the 0.25 μm CMOS process technology. The design steps are described, and a prototype was fabricated as a “proof of concept” for resistive mixer.

1.2 CMOS Technology

Several technologies can be used for designing radio frequency (RF) circuits, Bi-CMOS, GaAs, SiGe HBT, and Bipolar. But today, CMOS technology is the dominant semiconductor technology for integration of both analog and digital circuits on a single chip. CMOS circuits composed of NMOS and PMOS devices and provide the best speed per
power performance. In the digital circuits, unlike NMOS or bipolar circuits, CMOS circuit has the much smaller power dissipation and almost no static power dissipation. Power is only dissipated in case the circuit actually switches. This allows to integrate many more CMOS gates on an IC than in NMOS or bipolar technology, resulting in much better performance. Also it costs less than other technologies because of their lower fabrication costs and wafer costs. Due to the surge of faster digital processors, the gate length of a silicon device continues to decrease, making it possible to make small and high-speed RF circuits with CMOS and Bi-CMOS devices. Bi-CMOS devices on the same fabrication run, but it requires more mask and more processing cycles, making it more expensive than CMOS process. On the other hand, CMOS devices are cheaper, have a lower minimum noise figure, and better linearity than bipolar devices implemented in Bi-CMOS process. So CMOS technology is preferred for implementation of RF front-end circuitry [13].

In this thesis, design of a broadband mixer in the following CMOS process will be explored: TSMC 0.25 μm.

1.3 PMOSFET and NMOSFET

The characteristic of NMOSFET and PMOSFET are of prime importance in the performance analysis of analog applications of transistors and circuits fabricated with CMOS technology, because these transistors have different physical principles of operation.

Current through NMOSFET and PMOSFET transistors operated in linear region of passive mixers are given by the following equations (1.1).
When \( V_{gs} > V_{th} \) and \( V_{ds} > V_{th} \), the transistor is turned on, and channel has created which allows current to flow between source and the drain. The MOSFET operates as a resistor, controlled by gate voltage. The length and width is decided by the process in design. Electron mobility is dependent of doping concentration. Electron mobility is larger than hole mobility. In pure silicon electron mobility is approximately 2.5 or 3.0 times larger than hole mobility. PMOSFET with a P-doped channel between source and drain has greater series resistance and channel length reduction than an NMOSFET. Therefore PMOS transistors are often designed approximately 3 times wider width than a NMOS transistor, designed for the same current and voltage. PMOS offers lower Flicker noise, however NMOS offers a lower conversion loss.

Because of better performance of NMOSFET in mobility, the mixer using NMOSFET has more advantages in circuit size, the cost, high speed and linearity.

1.4 Objective and outline of thesis

The main objective of this thesis is to design a low cost, low conversion loss and high performance linearity broadband mixer and to examine different topologies of mixer.
and compare their performance on fabricated level.

Chapter 1 gives the motivation and outline to the thesis work.

Chapter 2 gives theoretical background for mixer before entering the design section.

Chapter 3 shows several different mixer topologies and compares them by simulation results. Design and simulation of the chosen mixer are presented in detail.

Chapter 4 shows the summary of the mixer's chip measurement.

Finally, in Chapter 5 gives the conclusions and future work.
Chapter 2

2. Theoretical Description

2.1 General Description

Mixer is a frequency converter which produces new frequencies different from those present in the input signal. Because any linear time-invariant systems cannot generate frequencies other than those present in the input signal, either time-varying or nonlinear systems are used as mixers [1].

\[
\begin{align*}
\text{IF} & \quad \rightarrow \quad \times \quad \rightarrow \quad \text{RF} = f_{\text{LO}} \pm f_\text{IF} \quad \rightarrow \quad \pm f_\text{IF} \\
\text{LO} & \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \quad \Rightarrow \quad \rightarrow \quad 2f_{\text{LO}} \pm f_\text{IF}
\end{align*}
\]

(a) \hspace{2cm} (b)

Fig. 2.1. Up-conversion and Down-conversion

Fig. 2.1 shows the property of frequency translation using the multiplication of two signals. In a transmitter application, the intermediate frequency \( f_{\text{IF}} \) and a local oscillator signal \( f_{\text{LO}} \) are mixed together to produce \( f_{\text{LO}} \pm f_\text{IF} \), and this is called up-conversion. In a
receiver application, an RF signal $f_{RF}$ and a local oscillator signal $f_{LO}$ are mixed together to produce an intermediate frequency $f_{IF}$, and much higher frequencies $2f_{LO} \pm f_{IF}$ are filtered out. This is called down-conversion mixer.

The principle of a mixer is based on using a multiplication between the RF signal and LO signal in the time domain to get the desired signal. This principle can be shown by the following trigonometric identity:

$$(A \cos \omega_1 t)(B \cos \omega_2 t) = \frac{AB}{2}[\cos(\omega_1 + \omega_2)t + \cos(\omega_1 - \omega_2)t] \quad (2.1)$$

From Fig. 2.1 we see that there is the product of difference frequency $(\omega_1 - \omega_2)$ at the mixer output. The amplitude of the product is proportional to the amplitude of the RF and the LO signals. The amplitude of the LO signal is constant so that the amplitude of IF is transferred from the amplitude of RF signal [3].

![Diagram](a) (b)

Fig. 2.2 Multiplication of two signals in time-domain.
Mixer changes only the center frequency with the information unchanged. Passing through the mixer, the baseband signal including the information is represented as the envelope and the LO signal as the center frequency as shown in Fig. 2.2 (b).

2.2 Active Mixer

Active mixers achieve conversion gain and require lower LO power than passive counterparts. Active mixers can be classified as unbalanced and balanced mixers. Balancing is a concept that depends on how the output signal is taken from the mixer. For the active mixers, the conversion gain is usually larger than 1, while it is always less than 1 for the passive mixers. A mixer with high conversion gain reduces the noise contribution from the subsequent stages. The distortion performance of the active mixers is worse than of the passive mixers. So there is a trade-off at distortion vs. gain, which exists between the passive and active mixers.

2.3 Passive Mixer

Passive mixers employ well known mixing techniques and excellent intermodulation performance at the expense of higher LO power. Passive mixers not using dc power supplies cannot amplify the input signal and so exhibit conversion loss. Passive mixer can be designed using diodes or MOSFETs. When used in passive mixers, MOSFETs operate as voltage switches (linear region of operation).
2.4 Unbalanced Mixer

The so-called unbalanced mixer is shown in Figure 2.3 and is the simplest of the active mixers. Port-to-Port isolation is a mixer concept that for example determines what fractions of the IF signal appears at the RF output. Feedthrough between different ports are undesirable in mixer design and can affect preceding or following circuits. It can be shown that the resulting components from mixing in the unbalanced mixer is both \((\omega_f t + \omega_{lo} t)\) and the unwanted \((\omega_{lo} t)\) frequency. This phenomenon is called IF-feedthrough and is undesirable.

![Fig. 2.3 Unbalanced mixer.](image)

2.5 Single Balanced Mixer

The single balanced mixer is an improvement over the unbalanced mixer but it also has its disadvantage. In this mixer structure the output is taken differential as shown in Figure 2.4. The signal is taken from two branches, therefore IF feedthrough from each branch cancels one another.
In this mixer the transistor of RF port always works in the saturation region. As shown, the RF signal is applied at the gate of the device of RF port so that it is converted to a current signal. The DC voltage of LO+ and LO- transistor are set around the threshold level. As the LO signal is applied, LO+ and LO- transistor will switch on and off in turn. While one of the LO transistor is on, the other is off. This requires the LO signal large enough to drive the complementary switch. In this case, the RF signal is multiplied by the LO signal. If we assume the LO signal is an ideal square wave, then the IF signal can be expressed as following:

\[ V_{IF}(t) = A_{IF} \cos \omega_{IF} t \times 2G \sum_{n=1}^{\infty} \frac{\sin \frac{n\pi}{2}}{n} \cos n\omega_{IF} t \]  

(2.3)

![Fig. 2.4 Single balanced mixer.](image)
The advantage of this structure is the rejection of RF feedthrough. As the IF signal is taken from both branches and follows the load resistors, the IF signal is derived from the difference of the two branches. So the RF feedthrough from both branches can cancel each other. On the other hand, the feedthrough of the LO signal will appear at the output [2].

2.6 Double Balanced Mixer

By the combination of two single balanced mixers, we can get the double balanced mixer, which is shown in Fig. 2.5

![Double balanced active mixer](image)

Fig. 2.5 Double balanced active mixer.

The nonlinearity and noise performance of the double balanced mixer are better compared to the single balanced mixer. But it consumes larger current than the single balanced mixer.
Compared to the single balanced mixer, the double balanced mixer can cancel the feedthrough of both the LO and the RF signal. But this only happens under ideal conditions. Actually, the mismatches at the RF or the LO port will cause some feedthrough.

**2.7 Gilbert Mixer**

The Gilbert mixer which is another type of the double balanced mixer has the advantages that it rejects both IF- and LO frequency components at the output. The mixer is shown in Figure 2.5. This kind of mixer is used in the design of the power mixer. The rejection of IF- and LO frequency components is under ideal conditions. In practice, there is always a little amount of feedthrough. The mixer contains a voltage to current converter which is composed of transistors RF+ and RF-. A difference in voltage is transformed to a difference in current through transistors RF+ and RF-. The currents i1f+ and i1f- generated from transistors RF+ and RF- are switched through the transistors LO+ and LO-. The ideal LO is a square wave. This square wave should be large enough to switch the transistors LO+ and LO- totally on when it is high and totally off when it is low [3].

**2.8 FET Resistive Mixer**

The passive FET mixer, normally called the FET resistive mixer, operates in the linear region, without any dc bias applied to the channel. The FET mixer uses the channel resistance. When no dc drain-to-source voltage is applied, each MOS transistor of Fig.2.6 operates in its linear region, as a switch. Each switch is driven between its “on” and “off”
states by applying the LO signal to its gate. The theoretical optimum conversion loss for an ideal balance passive mixer is equal to $20 \log(2) = -3.9\, dB$. The $\frac{2}{\pi}$ term is the ratio of the signal voltage to IF voltage. These assuming that LO signal at the gate is a square waveform and the $R_{on}$ resistance is zero, the RF and IF ports are conjugately matched, all intermodulation (IM) products are resistively terminated, and no parasitic resistive or reactive losses exist. The above analysis has been generalized to show that when matched loads are presented to each IM product, and the RF, IF, and image signals are conjugately matched. Also, when all IM products and the sum ($f_L + f_R$) product are reactively terminated, the IF is conjugately matched, and the RF and image signals are identically terminated, then the theoretical minimum conversion loss is 3 dB, with the lost energy equally divided between conversion to the image, and reflection-loss at the signal frequency [4],[12]. The advantages of such mixers are very low distortion, low $1/f$ noise, no shot noise and good isolation; the conversion loss of such mixers is comparable to diode mixers but the disadvantage is large LO power requirement.

![Fig. 2.6 Double balanced resistive mixer.](image)

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2.9 RF Mixer Design Parameters

2.9.1 Input and Output Impedance

In a super-heterodyne receiver, there is an off-chip image reject filter between the LNA and the mixer. Since the mixer input is connected to an off-chip component with a typical impedance of 50Ω, it needs to be matched to avoid reflections connecting image reject filter to the mixer. In a direct conversion receiver, there is no image reject filter between the LNA and the mixer, so the mixer is directly connected to the LNA output without going off-chip. However, since the mixer in this project is being designed without an LNA preceding it, the inputs would have to come from off-chip and the input needs to be matched to the source impedance that will drive it. The design assumes the input impedance (Z₀) is 50Ω, since this is the source impedance of almost all input sources. The input reflection coefficient (S₁₁) is a good measure of the input match. S₁₁ is defined as the ratio of the reflected wave voltage to the incident wave voltage at the input of the mixer and can be calculated using equation (2.3)

\[ S_{11} = \frac{Z_{in} - Z_0}{Z_{in} + Z_0} \]  \hspace{1cm} (2.3a)

\[ S_{11}(dB) = 20 \log |S_{11}| \]  \hspace{1cm} (2.3b)

For a perfect input match Zin = Z₀ = 50Ω. In most practical cases it is not necessary to have a perfect match. An S₁₁ < -10 dB, which corresponds to a reflection of less than 10%, is usually sufficient. The output of the mixer for a direct conversion receiver is at baseband so there is no need to match the output of the mixer to the load.
impedance. The load impedance of the mixer is the input impedance of the baseband channel selection filter.

### 2.9.2 Harmonics

The nonlinear system can be modeled using the following function:

\[
y(t) = a_1 s(t) + a_2 s'(t) + a_3 s''(t) \quad (2.6)
\]

Here \( y(t) \) is the output and \( s(t) \) is the input. The third-order polynomial specifies the third-order nonlinearity. Because of this nonlinearity, distortion is generated. Although there are many measures of nonlinearity, the most commonly used in RF design, are third-order intercept (IP3) and 1-dB compression point [2].

Using the function (2.6) with an input signal \( s(t) = A \cos \omega_0 t \), then the function of the output can be derived as:

\[
y(t) = \alpha_1 A \cos(\omega_0 t) + \alpha_2 A^2 \cos^3(\omega_0 t) + \alpha_3 A^3 \cos^3(\omega_0 t) \quad (2.7a)
\]

\[
= A \cos(\omega_0 t) + \frac{\alpha_2 A^2}{2}(1 + \cos(2\omega_0 t)) + \frac{\alpha_3 A^3}{4}(3 \cos(\omega_0 t) + \cos(3\omega_0 t)) \quad (2.7b)
\]

\[
= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right) \cos(\omega_0 t) + \frac{\alpha_2 A^2}{2} \cos(2\omega_0 t) + \frac{\alpha_3 A^3}{4} \cos(3\omega_0 t) \quad (2.7c)
\]

In the (2.7c) expression it can be seen that frequency components of \( \omega_0 t \), \( 2\omega_0 t \) and \( 3\omega_0 t \) are generated at the output. The \( \omega_0 \) component is called the fundamental frequency and the higher order terms are called "harmonics". Depending on how the
output is taken from the circuit different observations can be made. If the signal is taken out as differential, the even-order harmonics will vanish.

2.9.3 Third-order Inter-modulation Distortion

If two tones are applied to a mixer they will produce distortion at many different frequencies in the mixer’s output. Many of these components lie outside the desired signal band and are filtered out at some point in the receiver chain. However, some do appear in the signal band and cannot be filtered. If two input tones, at $f_1 + f_{LO}$ and $f_2 + f_{LO}$, are close in frequency the intermodulation components at $2f_2 - f_1$ and $2f_1 - f_2$ will be close to $f_1$ and $f_2$, making them difficult to filter without also removing the desired signal. These products are called third-order intermodulation (IM3) products. Figure 2.3 shows the frequency spectrums at the input and output of a typical mixer including the IM3 products.

The third-order intercept point is used to measure the intermodulation corruption. Since the desired signal is proportional to $A$ of $20 \log_{10} A$ in original tones and the third-order product is proportional to $A^3$ of $20 \log_{10} \frac{3A^3}{4}$ in third order products, this point is defined as the cross point of these two curves [6]. This is shown in the following Fig. 2.7 and Fig. 2.8.
Fig. 2.7 Frequency spectrum of a mixer.

Fig. 2.8 Graphical representation of the input and output third-order intercept point (IIP3, OIP3).
2.9.4 Second-order Inter-modulation Distortion

Second-order distortion performance is not critical in a mixer that is downconverting its input to an IF, since the second order products are out of the signal band. However, a mixer that is converting directly down to baseband has very stringent IIP2 requirements. To see why this is true, consider two interferers at $f_1 + f_{LO}$ and $f_2 + f_{LO}$ shown in Fig. 2.9. If $f_1$ and $f_2$ are approximately equal, their second order intermodulation products at $f_1 - f_2$ and $f_2 - f_1$ lie near DC, which is in the signal band.

![Diagram showing second order distortion in a direct conversion mixer.](image)

2.9.5 P1dB Compression Point

The P1dB is defined as the input or output signal level where the gain is decreased by 1 dB from its ideal value. Like IIP3, P-1dB is used to estimate the largest input that a mixer can handle. However, IIP3 is specified by extrapolating the first and third order curves from their values with small inputs, while P1dB is actually measured under large signal input conditions. It is straightforward to show that if the compression is caused exclusively by third-order nonlinearity the input P1dB is
\[ P_{1dB} = I_{IP} - 9.6dB \] \hspace{1cm} (2.8)

However, it is often the case that nonlinearities higher than third-order contribute to the gain compression or the supply headroom limits the output signal. Both of these cause (2.8) to be inaccurate.

![Graphical representation of the input P1dB.](image)

Fig. 2.10 Graphical representation of the input P1dB.

### 2.9.6 Flicker(1/f) Noise

The Flicker noise is inversely proportional to the frequency. The flicker noise is also called 1/f noise. The flicker noise associated with MOS devices is much more severe than that with bipolar devices, which has profound effect on analog integrated circuits, especially for narrow band direct conversion receivers. In a direct-conversion receiver, Flicker noise degrades the signal-to-noise ratio (SNR) and total noise figure (NF), which
results in the degradation of receiver sensitivity. The Flicker noise not only degrades the noise performance of mixers and phase noise of oscillators, but also adds noise directly to the base band [9]. PMOS has lower Flicker noise density than NMOS, possibly due to the fact that channel in PMOS is a little bit further away from the surface. Flicker noise is associated with the nature of MOS device and there is no effective solution today to decrease it.

2.9.7 LO Input Power

The purpose of the LO signal is to switch the mixer on and off. In order to operate properly, a mixer must be driven at the LO port by a sufficiently large LO signal. This signal's size is limited by the power delivered by the oscillator generating the LO signal.

2.9.8 LO Feedthrough

In a perfect mixer, the RF and LO signals would not be present at the IF port, and the LO would not be present at the RF port. In most receive mixers, it is important to have isolation between the LO and RF ports. Since the LO signal is usually a much stronger signal that the other two ports, a significant amount of it may leak to the mixers input and then leak back to the antenna through the reverse isolation of the LNA. This LO signal at the antenna will radiate out and can interfere with other nearby receivers. Also, LO (or RF) feedthrough signals at the IF port is that these signals may cause other spurious products later in the chain and decrease the P1dB of the mixer.
2.10 CMOS Circuit Design

2.10.1 MOS Transistor

Most popular technology for realizing microelectronic circuits makes use of MOS transistors. The MOS transistor is a device known as a FET, Field Effect Transistor. MOS stands for Metal-Oxide-Semiconductor which describes the gate, insulator and the channel region material. Today however, most MOS technologies utilize polysilicon gates rather than metal gates structure. The semiconductor material, used as the transistor starting material, is usually silicon and termed the substrate. There are two types of MOS transistors- NMOS and PMOS. The most commonly used symbols that are used for MOS transistors are shown in Fig. 2.12.

![Fig. 2.12 Symbols for NMOS(a) and PMOS(b) transistor.](image)
Most commonly used symbols for NMOS and PMOS transistors Fig. 2.13 shows a

cross section of a silicon NMOS transistor. Source (S) and drain (D) regions are heavily
doped n-type regions implanted into lightly doped p-type substrate. Between the drain
and source region silicon oxide is grown. A conductive material, most often
polycrystalline silicon (poly silicon), covers the oxide and forms the gate (G) of the
transistor. With no voltage applied to the gate, n+ drain and source regions are separated
by the p- substrate. The separation between those regions is called the channel length L.

For an NMOS transistor the source terminal is defined as the terminal that has a lower
voltage, while the definition is opposite for PMOS transistors. Applying a small positive
voltage to the gate causes positive carriers in the channel under the gate to repulse and a
deployment area is formed. A larger positive gate voltage attracts negative mobile carriers
from the source and drain regions and an n-channel is formed under the gate.

The NMOS transistor is a so called n-channel transistor where electrons are used to
conduct current, while holes are used to conduct current in the PMOS transistor. With
that, current flows from drain to source in a NMOS transistor and in the opposite
direction in a PMOS transistor, when turned on.
Fig. 2.13 Cross section of NMOSFET with off (a) and on (b) state.
Chapter 3

In this chapter, the design of PMOS and NMOS resistive ring mixers is described, including detailed simulation results. One NMOS and two PMOS mixers were designed and their layouts were implemented in TSMC 0.25μm process. The simulations were performed using Agilent ADS with BSIM3v3 and for layout work the Virtuoso layout tool from Cadence was used.

3. CMOS Ring Mixer Design

3.1 Schematic of Mixer

This mixer design is based on the basic structure of a resistive FET mixer. The four FET
ring mixer presented in Fig. 3.1 provides a double balanced solution with high linearity and good port to port isolation.

NMOS and PMOSFET under analysis for these mixer designs have the following technological parameters: gate oxide thickness of 57 angstrom, channel length of 0.24 \( \mu \)m, channel width of 240 \( \mu \)m and 660 \( \mu \)m, threshold voltage 0.48 of NMOS and 0.45 of PMOS. The mobility is 283.1 \( cm^2/V \cdot s \) for NMOSFET and 102.9 \( cm^2/V \cdot s \) for PMOSFET.

Fig. 3.2 Conversion loss of NMOSFET mixer as a function of device size without matching network.
In order to examine the conversion loss and Flicker noise differences between NMOSFET and PMOSFET mixers, three double balanced FET ring mixer were designed as following: each FET having a gate length and width of 0.24 and 240 μm for NMOSFET mixer, a gate length of 0.24 μm and width of 240 μm for PMOSFET mixer, and a gate length of 0.24 μm and width of 660 μm for PMOSFET mixer. The gate length was chosen equal to the minimum gate length of the TSMC 0.25 μm process. The main differences between NMOSFET and PMOSFET devices lead to different matching circuits and to a slightly different layout.

The first point during the optimization process of mixer design was the determination of the FET size with respect to RF matching and conversion loss. It has been found that both requirements can be fulfilled by a FET size whose impedance at the RF port matches with the real part of the normalized impedance and was used for the
determination of the matching elements. The MOS device size used for this circuit was chosen to yield the lowest conversion loss.

Without matching network at RF, LO and IF ports, the RF and LO signal with power of -40 and 13 dBm, respectively have been applied to the resistive FET mixer. Fig.3.2 and Fig. 3.3 illustrate the conversion loss for NMOS and PMOS device size at mixer design. In Fig.3.2, the NMOS device size at the mixer without matching network indicated the minimum value of conversion loss with device size of 240 $\mu$m whose value is 4.6 dB and in Fig. 3.3, the PMOS device size pointed to the minimum conversion loss with device size of 348 $\mu$m whose value is 5.65 dB. Even though the device size of 348 $\mu$m has minimum conversion loss at double balanced PMOSFET mixer, to compare the magnitude of Flicker noise between NMOS and PMOS devices, we choose same device size which is 240 $\mu$m and scaled for difference in mobility with NMOS resulting in 660 $\mu$m. PMOSFET must be wider to provide similar drain current as compared to NMOSFET. Typically the mobility of holes ($\mu_p$) is 2 time or 3 times lower than the mobility of electrons ($\mu_n$). After the device size for minimum conversion loss has been determined, the matching networks have been added.
Fig. 3.4 NMOSFET 240 schematic with matching network.

The matching networks of the NMOSFET with width of 240 μm in Fig. 3.2 have been designed with input frequency bandwidth of 1 to 3 GHz with a few passive elements. The RF and LO ports matching can be achieved using a single shunt inductance and a shunt resistance. This shunt resistor value of RF and LO ports was chosen to minimize RF power and LO power dissipation. RF and LO port impedances matched 50 Ω and IF port match to 50 Ω which match requirement removes the need to integrate large value IF matching components on-chip [7]. Also, IF ports include 10 pF capacitor to achieve better isolation between port and port. When joining the matching network for each port, to maintain circuit symmetry is important. If an asymmetry is introduced, the 180 degree out-of-phase balance is destroyed, and the LO to RF leakage degrades.
In Fig. 3.3 and 3.4, the PMOSFET mixer design with width of 240 \( \mu \)m and 660 \( \mu \)m have been designed with RF bandwidth of 1 to 3 GHz, RF power of -40 dBm and LO power of 13 dBm as NMOS mixer. IF frequency was fixed at 30 MHz.

Fig. 3.5 PMOSFET 240 schematic with matching network.
3.2 Mixer Performance

3.2.1 Return Loss

The figures 3.7 to 3.9 show the S-parameter and return loss simulation results of RF, LO and IF ports of three FET resistive mixers without matching network in bandwidth of 1 to 3 GHz, RF power of -40 dBm and LO power of 13 dBm, respectively. Without matching network, RF and LO ports of three FET resistive mixers do not have broadband return loss in RF frequency range of 1 to 3 GHz. But the IF ports of these three mixer show the excellent return loss below -15 dB with broad-bandwidth. IF port match to 50 Ohm which means that no matching network at IF port is needed on chip. The load impedance of the RF port of three resistive mixers is located inside the conductance unity.
(1 + jb) circle and the load impedance of LO port is located outside the resistance unity (1 + jx) circle and conductance unity circle.

Figure 3.7 The simulated return loss of NMOSFET 240 at RF, IF, and LO port, without matching network, respectively.
Figure 3.8 The simulated return loss of PMOSFET 240 at RF, IF, and LO port, without matching network, respectively.
Fig. 3.9 The simulated return loss of PMOSFET 660 at RF, IF, and LO port, without matching network, respectively.

Fig. 3.10 to 3.12 show the S-parameter and return loss simulation results of RF, LO and IF ports of three FET resistive mixers with matching network in bandwidth of 1.0 to 3.0 GHz, RF power of -40 dBm and LO power of 13 dBm, respectively. After adding the optimized matching network into each port of three resistive mixers, the return loss of RF and LO ports was achieved lower than -10 dB in the frequency range of 1.0 to 3.0 GHz, which demonstrates the broadband performance of the designed matching networks for these three mixers.
Fig. 3.10 The simulated return loss of NMOSFET 240 at RF, IF, and LO port, with matching network, respectively
Fig. 3.11 The simulated return loss of PMOSFET 240 at RF, IF, and LO port, with matching network, respectively
3.2.2 Conversion Loss

Fig. 3.12 The simulated return loss of PMOSFET 660 at RF, IF, and LO port, with matching network, respectively

Fig. 3.13 The simulated conversion loss of NMOSFET 240 as a function of RF frequency for LO power of 13 dBm.
Fig. 3.13 shows the conversion loss of NMOSFET 240 versus RF frequency in range 1 GHz to 3 GHz and IF frequency of 30 MHz, RF power of -40 dBm, LO power of 13 dBm. The conversion loss saturates at RF frequency of 1.9 GHz at 5.1 dB.

Fig. 3.14 and 3.15 show the simulated results of conversion as a function of RF sweep at IF frequency fixed of 30 MHz at PMOSFET 240 mixer and PMOSFET 660 mixer, respectively. A conversion loss of about 7.7 dB and 7.4 dB was achieved at the optimum frequency.

Fig. 3.14 The simulated conversion loss of PMOSFET 240 as a function of RF frequency for LO power of 13 dBm.
3.2.3 Input P1dB, IIP2 and IIP3

P1dB, Input IP3 and Input IP2 were simulated to examine the linearity of these three mixers.

Fig. 3.16(a) shows the 1 dB compression point at RF and IF frequency of 2.4 GHz and 30 MHz at NMOSFET mixer, respectively which is defined as the RF input power level that causes the conversion loss to increase by 1 dB. A P1dB input power compression point of about 8 dBm was achieved.

Fig 3.17 and 3.18 show the simulated results of P1dB compression point at RF and IF frequency of 2.4 GHz and 30 MHz at PMOSFET 240 mixer and PMOSFET 660 mixer with same configuration of NMOSFET 240, respectively. A P1dB input power compression point of about 9 dBm and 8 dBm was achieved, respectively.
Fig. 3.16 Input P1dB of NMOSFET 240, RF power: -40 dBm, LO power: 13 dBm, RF frequency: 2.4 GHz, IF frequency: 30 MHz.
Fig. 3.17 Input P1dB of PMOSFET 240,
RF power: -40 dBm, LO power: 13 dBm, RF frequency: 2.4 GHz, IF frequency: 30 MHz.
Fig. 3.18 Input P1dB of PMOSFET 660,
RF power: -40dBm, LO power: 13 dBm, RF frequency: 2.4 GHz, IF frequency: 30 MHz.
Fig. 3.19 IIP2 and IIP3 of NMOSFET 240, RF power: -40 dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.

Fig. 3.17 shows the third order inter-modulation behavior. Two RF tones with 2 KHz spacing are applied at the input of the mixer with equal power levels to perform input third order intercept point and input second order intercept point. All other parameters are as given in fig 3.20. An input third order intercept point (IIP3) of more than 7 dBm for NMOSFET 240 was achieved with LO power of 13 dBm.
Fig. 3.20 IIP2 and IIP3 of PMOSFET 240,
RF power: -40 dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.

Fig. 3.21 IIP2 and IIP3 of PMOSFET 660,
RF power: -40 dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.
3.2.4 Flicker(1/f) Noise

Fig. 3.22 to 3.24 show the flicker noise simulated in the frequency band of 3 to 100 Hz. These simulations show that using NMOS transistors for the mixer design lead to more 1/f noise than when PMOS devices are used.

Fig. 3.22 1/f noise of NMOSFET 240, RF power: -40dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.

Fig. 3.23 1/f noise of PMOSFET 240, Input RF power: -40 dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.
Fig. 3.24 1/f noise of PMOSFET 660, RF power: -40 dBm, LO power: 13 dBm, Input frequency: 2.4 GHz.

3.2.5 Port-to-Port Isolation

Fig. 3.25 Simulated LO - RF (a) and LO - IF (b) port isolation at RF frequency 2.4 GHz.
From the simulated LO to RF and LO to IF isolations with NMOS 240, PMOS 240 and PMOS 660 mixers. At NMOS 240 mixer, very high values of more than 54 dB in LO to IF isolation have been achieved at RF frequency of 2.4 GHz. Compared to the LO to RF isolation increased values of at least 19 dB can be observed.

### 3.3 Mixer Layout

The chip layout of the each mixer is shown in Fig. 3.26 to 3.28. The chip size of these mixers was designed with same size of 1.22 mm x 0.83 mm for convenience of measurement after fabrication. The chip was submitted for fabrication in standard 0.25 μm CMOS TSMC process. This CMOS process has 5 metal layers and 1 poly layer and uses deep n-well, thick top metal for inductor. The NMOS gate is fabricated on a p-type substrate. The drain and source are both n-plus doped regions, with the gate being composed of poly-silicon. The gate of NMOS and PMOS transistors is made of a N-doped polysilicon. The result is that the threshold voltages of NMOS and PMOS are not symmetric. The threshold voltage of NMOS and PMOS is 0.48 V and -0.45 V, respectively. One of PMOSFET mixer in these layouts uses device width about 2.5 times bigger than the NMOSFET, in order to keep the trans-conductance more or less equal. Also, in order to prevent latch-up, the source of both NMOS and PMOSFET are connected to their respective substrate regions. The high sheet resistance of the poly-silicon layer in the MOS transistors could degrade mixer conversion loss, the parasitic series resistance within the device was considered to minimize in the layout [8].

The NMOS transistors in this mixer have the total device gate width of 240 μm which is arranged to minimize the gate series resistances by separating into 20 multiple
fingers that each one has a size of 12 μm. Also, terminal to terminal and substrate to terminal parasitic capacitance have to be taken into account. The PMOS devices in Fig.3.24 have the same configurations as NMOS ones. The PMOS devices in Fig.3.25 have the gate width of bigger size than NMOS devices, which have total gate width of 660 μm with separated 55 multiple fingers.

Planar spiral inductors are probably the most commonly used and discussed in layout process. Low quality factor (Q) of these inductors can significantly degrade circuit performance in mixer. For layout of this process, five metal levels are available with 2 μm thick top level metal for improved inductor Q value in this process. Planar spiral inductor Q value for inductance of 1- 6 nH are around 6 in RF frequency bandwidth. Measured inductance and Q values for 1nH, 3nH and 6nH inductors are shown in Fig.3.22.

![Fig. 3.26 Measured inductance and Q values for 1 nH, 3nH and 6 nH planar spiral inductors.](image)
Fig. 3.27 Layout of NMOSFET 240 mixer,
Chip size is 1.22 mm x 0.83mm.

Figure 3.28 Layout of PMOSFET 240 mixer,
Chip size is 1.22 mm x 0.83mm.
Fig. 3.29 Layout of PMOSFET 660 mixer at level 0 in Cadence Virtuoso.
Chip size is 1.22 mm x 0.83 mm.
Chapter 4

4. Measurement Results

The chip was submitted for fabrication in standard 0.25 μm CMOS TSMC process. All on wafer measurements were carried out with an LO power of 13 dBm and RF power of -40 dBm without gate bias. The IF frequency was set to 30 MHz in all measurements.

4.1 How to Measure

The mixers were characterized using a probe station with differential probes of SGSGS on RF and on LO ports, and at IF port, one IF port was terminated with 50 and the other port was connected to spectrum analyzer or network analyzer. For adaptation of the balanced structure to the single ended RF and LO signal sources two 180 degree hybrids have been used while testing the chip.

WinCal and HP 8510 vector network analyzer will be used to extract for the scattering parameters of the three CMOS resistive passive mixers. Also, for FET resistive mixer, one spectrum analyzer for IF port and two signal generator for RF port and LO port are used to measure the conversion loss versus frequency and the P1dB compression point. To measure the Input Third Order Intercept Point (IIP3) and the Input Second Order Intercept Point (IIP2) in two tones test, one spectrum analyzer for IF port and two signal generator for RF port and one signal generator for LO port are used. When measuring LO-RF or LO-IF isolation, requiring 50Ω termination at unused ports, 50Ω
termination is connected to the IF port or RF port and the power at the RF port and IF port is measured to obtain the isolation performance with pumped LO power of 13 dBm.

Fig. 4.1 Mixer measurement system.

4.2 Summary of Measurements

4.2.1 Return Loss

The measured return loss as a function of RF for each mixer looking at RF, LO and IF ports are shown in Fig. 4.1 to 4.6. As can be noticed from the figures in 4.1(a) to 4.2(b), a return loss better than -10 dB over the RF bandwidth of 1 GHz to 6 GHz and over the LO frequency bandwidth of 1.5 GHz to 4.8 GHz, respectively has been achieved for the NMOS 240 mixer, which demonstrates the broadband performance of the designed matching networks. The match at the output port is also better than -10 dB from dc up to 100 MHz in figure 4.2(a). In Figure 4.2(b), increased LO power up to 20 dBm resulted in
even better IF return loss value of -25 dB and wider frequency range from DC to 100 MHz.

Fig. 4.2 Measured return loss at RF and LO port of NMOSFET 240 as a function of RF frequency.
Fig. 4.3 Measured return loss at IF port of NMOSFET 240 as a function of RF frequency.

The Figures 4.3 and 4.4 show the measured return loss better than -10 dB over the RF bandwidth of 1 GHz to 6 GHz and over the LO frequency bandwidth of 1.2 GHz to 4.2 GHz, and RF bandwidth of 1.2 GHz to 3.2 GHz and over the LO frequency bandwidth of 1.0 GHz to 3.0 GHz, respectively has been achieved for the PMOS 240 and the PMOS 660 mixer. The measured return loss at the IF port is shown in figure 4.4 (a) and 4.6(a). For the frequency range of DC to 40 MHz a conversion loss of below -6 dB was measured with LO power of 13 dBm. The figure 4.4(b) and 4.6(b) show that return loss of IF port with below -15 dB and -20 dB in the frequency range of DC to 40 MHz, respectively when LO power of 20 dBm are pumped.
Fig. 4.4 Measured return loss at RF and LO port of PMOSFET 240 as a function of RF frequency.
Fig. 4.5 Measured return loss at IF port of PMOSFET 240 as a function of RF frequency.
Fig. 4.6 Measured return loss at RF (a) and LO port (b) of PMOSFET 660 as a function of RF frequency
Fig. 4.7 Measured return loss at IF port of PMOSFET 660 as a function of RF frequency.
4.2.2 Conversion Loss

Fig. 4.8 Measured conversion loss versus available LO power of NMOSFET 240,
RF power -40 dBm, gate bias voltage = 0, 0.2, 0.45, 0.6 V,
RF frequency = 2.4 GHz, LO frequency = 2.37 GHz, IF frequency = 30 MHz.

Fig 4.7 demonstrated the relationship between conversion loss and LO power as a function of gate bias voltages when RF power is fixed at -40 dBm. As can be seen from the figure, by applying a small gate bias voltage, the increased gate bias voltages by 0.6 V (slightly higher than the threshold voltage of this transistor) can be achieved the better conversion loss for low level LO power.

A measured conversion loss of 63 dB and 10.1 dB is achieved for a 2.4 GHz input signal to the output using 0 dBm and 13 dBm of LO power without gate bias, respectively. It can be seen clearly that much lower conversion loss is possible if higher LO drive are pumped. Conversion loss values down to 10 dB are possible. The difference between the
measured and simulated conversion loss results from the variation between the fabricated transistor parameters and the model used in simulation.

Fig. 4.9 Measured conversion loss versus RF frequency of NMOSFET 240, available LO power 13 dBm, RF power -40 dBm, IF frequency = 30 MHz, gate bias voltage = 0, 0.2, 0.45, 0.6 V.

Fig. 4.10 Simulated conversion loss versus RF frequency of NMOSFET 240, available LO power 13 dBm, RF power -40 dBm, IF frequency = 30 MHz, gate bias voltage = 0, 0.2, 0.45, 0.6 V.
The mixer conversion loss plotted as a function of the RF frequency given LO power 13 dBm, RF power -40 dBm with gate biased voltage from 0 to 6 V, and downconverted output signal at 30 MHz is shown Fig.4.8. As can be seen in the figure, the conversion loss of NOMS 240 have the lowest value at the small DC gate biased voltage of 0.6 V, which has a conversion loss of 7.8 dB. Without gate bias, the conversion loss increased to 10.1 dB at 2.0 GHz of input signal.

![Conversion loss versus RF frequency of PMOSFET 240 and 660. Available LO power 13 dBm, RF power -40 dBm, gate bias voltage 0 V, and IF frequency 30 MHz.](image)

The mixer conversion loss of PMOS 240 and PMOS 660 plotted as a function of the RF in range 1 GHz to 4 GHz given LO power 13 dBm, RF power -40 dBm without gate biased voltage, IF port signal at 30 MHz is shown Fig. 4.9. As can be seen in the figure, the conversion loss of POMS 240 and PMOS 660 mixer has the lowest value of 21.8 dB and 14.8 at 2.4 GHz of optimum signal, respectively.

Figure 4.10 shows the conversion performance of the PMOS 660 mixer measured with RF frequency of 2.4 GHz, IF fixed at 30MHz and without gate bias while sweeping
the LO power level from 0 dBm to 20 dBm. Better conversion loss of approximately 14 dB can be achieved down to 20 dBm LO power.

Fig. 4.12 Conversion loss versus LO power of PMOSFET 660, available RF power -40 dBm, gate bias voltage = 0 V, RF frequency = 2.4 GHz, LO frequency = 2.37 GHz, IF frequency = 30 MHz.

4.2.3 Input P1dB, IIP2 and IIP3

Fig. 4.11 show the measured P1dB compression point for one NMOS mixer and two PMOS mixers at RF frequency of 2.4 GHz, IF fixed at 30MHz, RF power of -40 dBm, LO power of 13 dBm, respectively. P1dB input power compression point occurs at 7 dBm, 17 dBm and 14 dBm of input power in NMOS 240, PMOS 240 and PMOS 660 mixer, respectively.
Fig. 4.13 The measurements results of each mixer on P1dB.

Fig. 4.14 The third order inter-modulation components.

The IIP3 measurement value of the NMOS and PMOS resistive mixers when the two tones of 2.401 and 2.399 GHz in RF frequency were mixed with an LO frequency of 2.37 GHz with LO power of 13 dBm and RF power of -40 dBm. Resulting in IF signal at 29.999 and 30.001 MHz and the third order intermodulation at 29.997 and 30.003 MHz. Table 4.1 are listed the calculated and measured IIP3 results which shows that IIP3 of each mixer is 12 dBm in NMOS 240, 7 dBm in PMOS 240, 17.25 dBm in PMOS 660. Comparing with simulation results, the value is not much lower from simulation values.
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<td>IIP2 [dBm]</td>
<td>45.49</td>
<td>41.33</td>
<td>36.49</td>
</tr>
</tbody>
</table>

(b)

Table 4.1 The measurement results of P1dB, IIP2 and IIP3.

4.2.4 Flicker(1/f) Noise

The Flicker noise associated with MOS devices is much more severe than that with bipolar technology. However FET resistive mixers exhibits lower levels of 1/f noise than diode or active mixers, because of low surface-state density than diode and no gate bias, lower current flow of switching stages and the periodic switching of the transistor [10].

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The Flicker noise has strong dependence on gate bias and surface-state density [11]. Flicker noise investigations under switching conditions were performed from 3 Hz to 100 Hz of the measurement system. As seen in the measurement, NMOSFET mixers have higher 1/f noise than PMOSFET mixers.

The physical size and ON resistance of the mixer, the mean DC offset level of the LO signal, the parasitic capacitance and the LO frequency are all important in determining the noise performance.

Fig. 4.15 1/f noise of NMOSFET 240.
Fig. 4.16 l/f noise of PMOSFET 240.

Fig. 4.17 l/f noise of PMOSFET 660.
4.2.5 Port-to-Port Isolation

Fig. 4.18 Measurement system for LO to RF port isolation.

Fig. 4.19 Measurement system for LO to IF port isolation.
Isolation is defined as the attenuation in dB between a signal input at any port and its level measured at any other port. In the down-conversion mixer, the isolation between LO and RF ports of the mixer is important because LO to RF feedthrough results in LO signal leakage through the antenna. Also, large LO and RF feedthrough signals at the IF output port may saturate the IF output port, and decrease the $P_{1dB}$ of the mixer [13].

Fig. 4.20 Measured LO – RF (a) and LO – IF (b) port isolation at RF frequency 2.4 GHz.

Fig.4.16 and Fig.4.17 illustrate how to measure LO to RF and LO to IF isolation. When measuring LO to RF isolation, a 50 ohm termination is connected to the two IF ports and the one RF port, the LO power at the RF port is obtain the isolation performance. Also, when measuring isolation from LO to IF, the power applied at the LO port and a 50 ohm termination is connected to the one IF ports and the two RF ports, the LO power at the IF port is measured the isolation performance. Fig.4.18 shows the measured results of the LO to RF and LO to IF isolation performance at the RF of 2.4 GHz.
GHz for each MOSFET mixers with RF power of -40 dBm and LO power of 13 dBm, respectively. At NMOS 240, PMOS 240 and PMOS 660 mixer, very high isolation value of 50.5 dB and 58 dB, 48.5 dB and 56.0, 45.5 dB and 54.76 dB were obtained for both LO to RF and LO to IF measurement, respectively.

<table>
<thead>
<tr>
<th>Name</th>
<th>Using non-ideal element (Inductor)</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF Port</td>
<td>1.00 - 3.00</td>
<td>[GHz]</td>
</tr>
<tr>
<td>LO Port</td>
<td>0.97 - 2.97</td>
<td>[GHz]</td>
</tr>
<tr>
<td>IF Port</td>
<td>30</td>
<td>[MHz]</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Device</th>
<th>Conversion Loss</th>
<th>Simulated results</th>
<th>Measured results</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOSFET</td>
<td>5.1 to 5.9</td>
<td>7.7 to 9.8</td>
<td>8.1 to 10.9</td>
</tr>
<tr>
<td>PMOSFET</td>
<td>7.4 to 9.4</td>
<td>9.4 to 9.4</td>
<td>24.8 to 28.8</td>
</tr>
<tr>
<td>PMOSFET</td>
<td>8.1 to 10.9</td>
<td>19.8 to 24.8</td>
<td>12.8 to 28.8</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>LO to RF Isolation</th>
<th>35.1</th>
<th>33.8</th>
<th>30</th>
</tr>
</thead>
<tbody>
<tr>
<td>LO to IF Isolation</td>
<td>54.6</td>
<td>53.5</td>
<td>43.9</td>
</tr>
</tbody>
</table>

Table 4.2 summarizes the simulated and measured results for three MOSFET mixers.
5. Conclusion and Future Work

5.1 Conclusions

This thesis work has presented the performance of three CMOS resistive mixers, one NMOSFET mixer and two PMOSFET mixers built in 0.25 μm CMOS TSMC process. It has demonstrated 10.1 dB minimum conversion loss in NMOSFET of width 240 μm, 12 dBm IIP3 and 7 dBm P1dB, in PMOSFET of width 240 μm conversion loss of 21.8 dB, 7 dBm IIP3 and 17 dBm P1dB, in PMOSFET of width 660 μm conversion loss of 14.8 dB, 19.25 dBm IIP3 and 14 dBm P1dB, when the consuming no DC power, respectively. The overall performance makes the mixers well suited for both, direct conversion and heterodyne architectures, offering a wide range of applicability. The performance highlights are: no DC power consumption, high linearity and port-to-port isolation, and low 1/f noise.

5.2 Future Work

Conversion loss of these mixers could be improved in all mixers by using different inductor layout model. The inductor models used in this mixer design have relatively small center holes that make shift of center frequency to higher frequency, from the results optimum conversion loss in the range 1 GHz to 3 GHz could not achieved. In these mixer designs, eight spiral inductors at NMOS 240 and PMOS 240 and ten inductor models at PMOS 660 mixer, respectively were used to implement the matching network.
which could be made worse conversion loss with ohmic and substrate loss. The spiral inductor layout could be further optimized so reduce area and parasitic parameters.
References


July 1999.


