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MMIC AlSb/InAs HEMT Grid Oscillator for Millimeter-Wave Operations

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Abstract

The AlSb/InAs high electron mobility transistor (HEMT), a novel III-V material electronic device, has the advantage of low noise, low-power consumption, and high-frequency operation. However, its low available output power limits its applications. To fully exploit the advantage of this device at millimeter-wave frequencies, quasi-optical power-combining techniques are used in this thesis to overcome this power limitation.

A MMIC grid oscillator using AlSb/InAs HEMTs on a GaAs substrate was designed using a unit-cell approximation and two-port network model. Loop analysis predicted a 50-GHz operational frequency. The equivalent circuit required for maximum output power was synthesized with the approximated large-signal S-parameters, and the corresponding optimum circular function indicates that the designed grid oscillator works at under-compression point. The substrate mode associated with this grid was analyzed, and negative impact is shown to the E-plane radiation pattern.

A 4 × 4 and a 6 × 6 array of MMIC grid oscillators based on the design were fabricated and tested. Unfortunately, due to the unresolved fabrication issues at the foundry, the RF performance could not be evaluated. In addition, a 6 × 6 array of C-band hybrid grid oscillator was designed, fabricated and tested. It was found that edge effects had an impact on the oscillation frequency, EIRP, and DC-RF conversion efficiency.

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Chapter 1 Introduction

The reduction of available spectrum due to increased demand in wireless communication has driven expansion into the millimeter and sub-millimeter-wave range, between 30 GHz - 3 THz. Circuits built for this range have advantages of smaller and lighter components as well as larger bandwidth than microwaves. The development of solid-state devices in the frequency range greater than 100 GHz has made millimeter and sub-millimeter-wave systems among the most active research areas with strong industry demand and rapid technological advances.

1.1 High-Frequency Operation

Wireless communication systems are migrating towards higher data rates, but this is largely limited by the bandwidth of a point-to-point communication channel. Therefore, increasing the bandwidth is a convenient way to achieve high data rates.

Unfortunately, most bands within the frequencies that have favorable propagation properties (low-GHz range) have already been allocated [1]. To solve this problem, unlicensed Industrial-Scientific-Medical (ISM) bands have been widely used. However, squeezing more applications into these crowded ISM bands causes interference.

Therefore, moving to higher frequencies seems like a natural solution due to more available bandwidth. For example, the unlicensed band at 60 GHz can provide 5 GHz bandwidth (59-64 GHz), which is significant compared to the ISM bands at 2.4 GHz (80 MHz) or 5.8 GHz (150 MHz) [1]. However, this presents a challenge to

circuit designers, who must achieve high-frequency operation and enough usable power at the same time.

1.2 Quasi-Optical Power Combining

The requirement of high frequency/high speed and wide bandwidth is driving wireless communication into the millimeter-wave range. Compared to microwave systems, millimeter-wave systems have wider bandwidth and reduced size and weight. Compared with optical systems, millimeter waves have the advantage of penetrating smoke, fog, and dust. At the same time, the development of new solid-state devices with high operating frequencies makes them promising for millimeter-wave systems.

However, while solid-state devices have the advantage of size, weight, reliability, manufacturability, and DC requirement, their power-handling capacity is reduced in the millimeter-wave region. Figure 1.1 [2] compares the average power of representative solid-state and vacuum electronic devices. It shows that the power of solid-state devices tend to fall off with a $1/f$ to $1/f^2$ frequency dependence.

To exploit the advantage of solid-state technology for useable power levels at millimeter-wave frequencies, the power from multiple solid-state components must be added coherently. Techniques for device- and circuit-level combining based on conventional circuits [3]-[5], such as parallel or corporate with binary Wilkinson power combiners, provide solutions to some extent. However, they approach fundamental limits in device power density and combining efficiency, since

combining a large number of devices will complicate the circuitry and transmission losses are excessive.

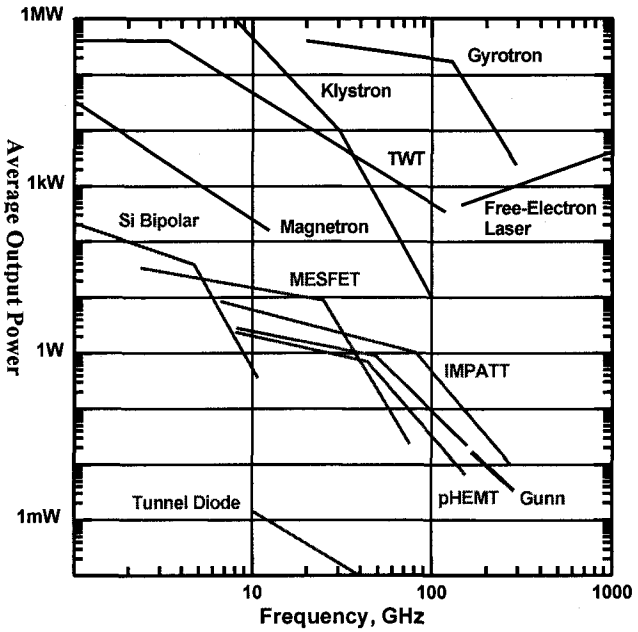

Fig. 1.1 Power handling capacity from a variety of millimeter-wave sources [2].

To address this problem, recent research has concentrated on developing power combiners using quasi-optical methods [6]-[8] which can integrate large numbers of devices with minimal signal distribution and combining losses as well as maintain desired amplitude and phase relationships.

In a quasi-optical power combiner, an array of solid-state devices is distributed over a planar radiating structure and interacts directly with an electromagnetic beam. It provides enhanced RF efficiency by coupling the active components to large-diameter guided beams or waveguide modes, rather than the planar transmission lines used in circuit-combining structures.

Since 1986, when Mink first proposed quasi-optical power combining techniques [9], quasi-optical applications have expanded from just power generation to various circuits such as amplifiers, mixers, phase-shifters, switches, frequency multipliers, modulators, and beam-steerers [6]. All of these quasi-optical circuits provide the following advantages:

- Overcome the limited power problem encountered by using solid-state device at high frequencies, such as millimeter-wave range, since many low-power devices can be spatially combined with minimal loss.
- Tune gain and power independently. Since the impedances seen by the active devices is primarily determined by the array's unit cell, while the output power scales with the total number of devices, the gain can be optimized through the unit cell and the system power requirement can be met through the array size independently.
- Compact, lightweight, and amenable to monolithic integration, since the antenna is integrated into the circuit. For example, the antenna serves as a part of the feedback to the oscillator or amplifier. This eliminates the feed lines, and therefore reduces the size of the circuit.
- Acceptable noise figure since the noise adds incoherently, even though the total power adds coherently.
- High reliability. Since the total output power is the added by the power from individual device, a degradation of the circuit due to the failure of a fraction of the devices will appear instead of sudden failure of the whole circuit.

1.3 Grid Oscillators

Grid oscillators are quasi-optical power combiners which have been demonstrated at both microwave and millimeter-wave frequencies [10]. A grid oscillator converts DC power into RF power as well as efficiently radiates the RF power into free space.

Figure 1.2 shows the schematic of a grid oscillator. Basically, it consists of an array of solid-state devices embedded in a metal grating which is supported by a dielectric substrate. The horizontal lines of the grid serve as DC bias lines, and the vertical lines as antennas, on which RF currents cause an electromagnetic wave to be radiated away from the grid. The mirror, substrate, and grid dimensions are chosen to provide positive feedback for the oscillation. Sometimes a partially transparent reflector is placed in front of the grid for tuning. An oscillation is triggered by noise or transients on the DC bias.

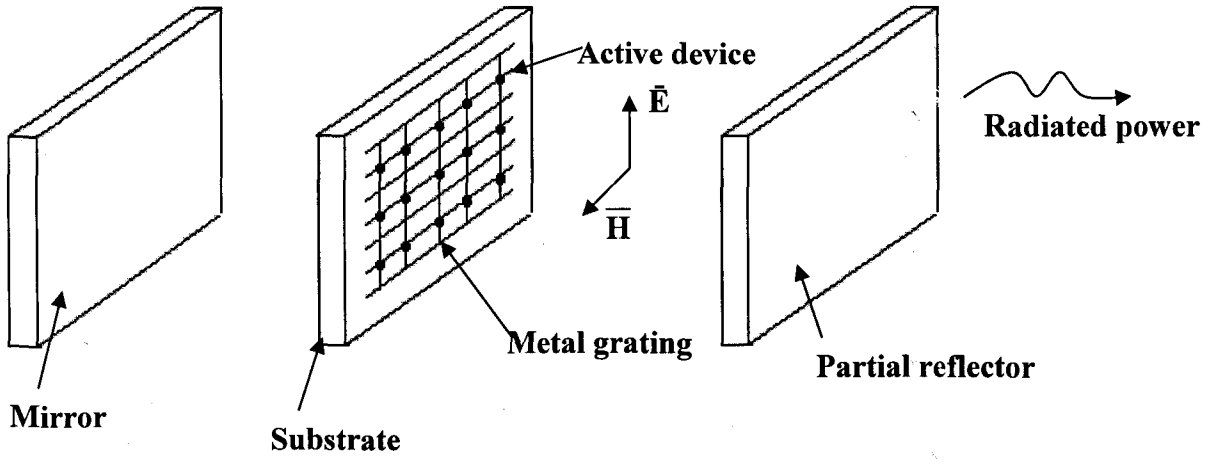

Fig. 1.2 Schematic of a grid oscillator. An array of active devices embedded in a metal grating is placed in a Fabry-Perot cavity. [10]

Since the first quasi-optical oscillator was developed by Popovic *et al.* in 1988 [10], a number of grid oscillators have been demonstrated [10]-[20]. Grid oscillators reported before 1997 are summarized in reference [10], and fall into one of the following categories: (a) the prototype grids, (b) grids designed for higher frequencies, (c) grids designed for added capabilities, and (d) grids designed for optimizing output power. Since 1997, extensive effort has been devoted to increasing the output power [12]-[14] and functionality [14]-[19] of grid oscillators. Only one paper dealt with high-frequency grid oscillators with the highest reported frequency at 43 GHz [20].

It has been shown [9], [13], [19] that grid oscillators for high operational frequency can be fabricated either by hybrid-circuit techniques in which the active devices are mounted on the surface of a dielectric substrate, or monolithic integrated-circuit techniques. Compared with hybrid circuits, monolithic fabrication of a grid has the advantage of smaller size, lighter weight and higher operating frequency. It also eliminates the problem inherent in hybrid-circuit techniques - as the number of elements on the grid increases, mounting the devices on the substrate becomes a difficult and tedious process. As the size of solid-state devices reduces with their operating frequency entering millimeter-wave region, this problem is more apparent in hybrid-circuit techniques.

1.4 Objective and Organization of the Thesis

The main objective of this thesis is to design the first MMIC AlSb/InAs HEMT grid oscillators at 50 GHz and deal with the power optimization and substrate-mode minimization in these grid oscillators.

Chapter 2 reviews grid oscillator analysis techniques. The unit cell approximation, two-port network model, and circular function are discussed. Oscillation criteria are presented. Two CAD software applications, High Frequency Simulation Software (HFSS) and Advanced Design System (ADS), are used to analyze grid oscillators.

Chapter 3 presents the design of a C-band hybrid grid oscillator based on the techniques discussed in Chapter 2. The fabrication and measurement results of this grid oscillator are also shown.

Chapter 4 presents the design of Q-band MMIC AlSb/InAs HEMT grid oscillators first. Then the feedback-optimization based on an equivalent circuit model and the large-signal S-parameter approximation are studied for this grid. After this, the substrate modes properties, such as the number of guided substrate-modes and the substrate-mode power, are investigated from an electromagnetic analysis. Finally, the experimental results of a 4×4-arry and a 6×6 array of MMIC AlSb/InAs HEMT grid oscillators designed for 50 GHz are shown, and the failure reasons are discussed.

Finally, Chapter 5 summarizes the major work of this thesis and provides suggestions for future work.

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Chapter 2 Analysis of Grid Oscillators

This chapter reviews the analysis of grid oscillators. In the analysis of grid oscillators, the passive part (e.g., the grid) and the active device are modeled as separate two-port networks. Then the circuit consisting of the passive network and active network is examined to determine if it satisfies the oscillation condition. Section 2.1 focuses on the unit-cell approximation and feedback-oscillator model consisting two-port networks. Section 2.2 discusses the oscillation condition using the two-port network model and circular function.

2.1 Analysis of Grid Unit Cell

A rigorous analysis of grid oscillators is a very complicated and difficult task due to the mutual coupling between the array elements and the edge effect of the grid. To simplify the problem, grid oscillators are often analyzed by assuming that the grid consists of an infinite number of repeated identical unit cells in which the embedded devices oscillate at the same frequency and phase. This is called the *unit cell approximation*. Based on these assumptions, the analysis of a whole grid oscillator reduces to a unit cell.

In a unit cell, the passive part, i.e., the metal grating, substrate, mirror, and free space, can be characterized by the induced EMF [1] or full-wave [2] analysis, by treating the unit cell as an equivalent waveguide, shown in Fig. 2.1, which contains a current source and has electric walls on the top and bottom and magnetic walls on the sides. This model arises from image theory in which the electromagnetic field

boundary conditions allow the horizontal symmetry bias lines to be replaced with electric walls and vertical symmetry lines between adjacent devices to be replaced with magnetic walls.

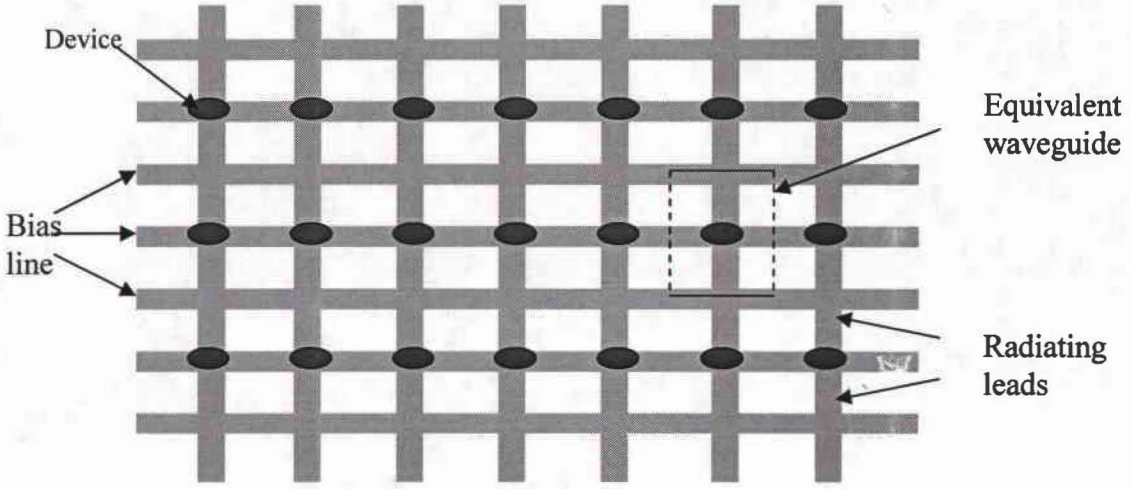


Fig. 2.1 Diagram of an active device array showing the equivalent waveguide unit cell. The active device (current source) sits in the center of each unit cell. The top and bottom of waveguide are electrical walls (solid line). The sides are magnetic walls (dashed line). [3]

The passive grid can be represented in a two-port network with a set of characteristic S-parameters. Similarly, the active device of the unit cell can be characterized with a set of two-port S-parameters. In both two-port networks, one port represents the gate-source port, and the other represents the drain-source port, in this thesis. The unit-cell grid oscillator can be modeled as a circuit consisting of a feedback two-port network (metal grating, dielectric substrate, mirror, and free space) and an active two-port network (transistor), as shown in Fig. 2.2.

For this closed-loop circuit, circular-function analysis will be applied to examine the potential for oscillation.

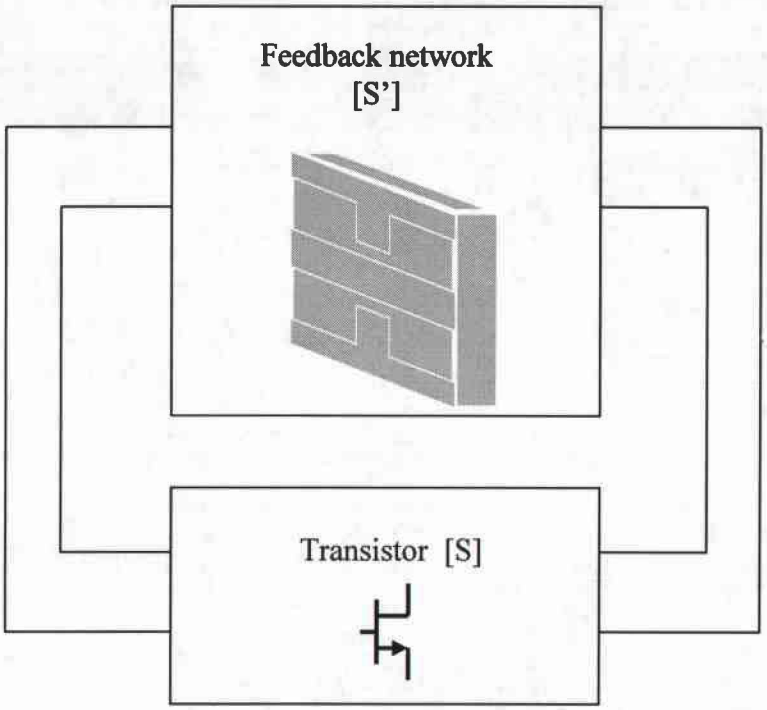


Fig. 2.2 Feedback-oscillator model of a grid oscillator unit cell, consisting of the two-port active network (transistor) and the two-port feedback network (passive grid). [4]

2.2 Circular Function

Whether a circuit oscillates or not depends on it satisfying the oscillation criterion. The generalized steady-state oscillation condition [5] of an n-port feedback oscillator is

$$\det([\mathbf{S}][\mathbf{S'}] - [\mathbf{I}]) = 0 \tag{2.1}$$

where [S] and [S'] are the n-port scattering matrices of the active devices and embedding networks, respectively, and [I] is the identity matrix.

For the case of n = 2, this equation simplifies as

$$S_{11}S_{11}^{'} + S_{12}S_{21}^{'} + S_{21}S_{12}^{'} + S_{22}S_{22}^{'} - |\mathbf{S}||\mathbf{S}^{'}| = 1 \tag{2.2}$$

where

$$|\mathbf{S}| = S_{11}S_{22} - S_{12}S_{21}$$

and

$$|\mathbf{S}'| = S'_{11}S'_{22} - S'_{12}S'_{21}$$

For this case, the oscillator can be represented as two two-port networks - active device and feedback network, connected together. To perform the simulation, the circuit is broken at some point and a test probe is inserted at this point to evaluate the loop gain as shown in Fig. 2.3 (a) [6].

In the circular-function method [7], the probe, a circulator, is expressed as

$$[\mathrm{S}''] = \begin{bmatrix} S''_{11} & S''_{12} & S''_{13} \\ S''_{21} & S''_{22} & S''_{23} \\ S''_{31} & S''_{32} & S''_{33} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

To determine the loop-gain with the circulator in Fig. 2.3 (a), a signal flow graph is drawn, and Mason's rule [8] is applied to it. As a result, the loop gain, called the *circular function*, is given by:

$$C = \frac{S_{11}S'_{11} + S_{21}S'_{12} - |\mathrm{S}||\mathrm{S}'|}{1 - S_{12}S'_{21} - S_{22}S'_{22}} \tag{2.3}$$

At steady-state, the oscillation condition is $C = 1\angle 0°$, which is (2.2) for the case of n = 2.

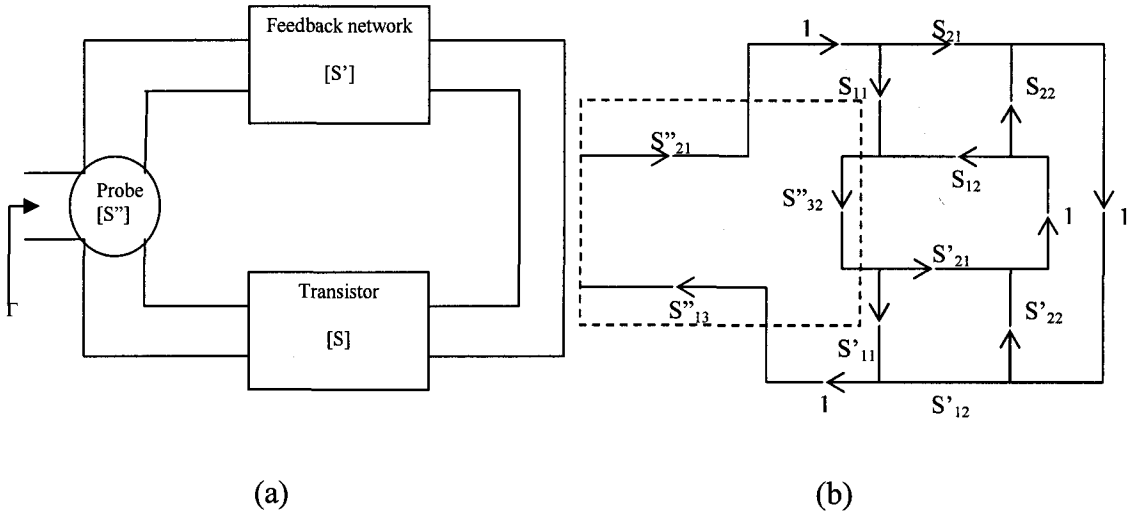


Fig. 2.3 (a) A two-port feedback oscillator with a probe, and (b) the signal flow graph of the circular function method. [6]

$C = 1\angle 0°$ guarantees sustained oscillations in a mathematical sense. It is well known, however, that the parameters of any physical system cannot be maintained constant forever. For example, if somehow the magnitude of C becomes slightly less than unity, oscillation will cease. In contrast, if the magnitude of C exceeds unity, oscillation will grow in amplitude. Therefore, a gain-controlled mechanism is needed for forcing C to remain equal to unity at the desired value of output amplitude.

Basically, the function of the gain-controlled mechanism works as follows. First, to ensure that oscillation will start, the circuit is designed so that the magnitude of C is slightly greater than unity and phase of C is 0 degree. Thus as the power supply is turned on, oscillations will grow in amplitude. When the amplitude reaches the desired level, the nonlinearity comes into action and causes the loop gain to be reduced to exactly unity. This will cause the circuit to sustain oscillations at this desired amplitude. Usually, the nonlinearity is realized by an element whose resistance can be controlled by the amplitude of the output sinusoid, such as BJT or FET transistors.

Therefore, to start the oscillation, it is required that $|C| > 1$ and $\angle C = 0°$. On a polar plane, the circular function C can be plotted as a function of the frequency. It is easy to determine whether an oscillation occurs by examining if a frequency crosses the $\angle 0°$ line.

2.3 Simulation of Grid Unit Cell

For a grid oscillator designed to oscillate at a certain frequency, the active device and the grid geometry (substrate dielectric constant and thickness, unit cell size and mirror spacing) have to be properly selected to satisfy the oscillation condition, e.g. $|C| > 1$ and $\angle C = 0°$ for oscillation start-up, and $C = 1\angle 0°$ for steady-state, at that frequency.

To aid the grid unit cell design, a moment-method-based program called GAP has been used [2]. For a given dielectric substrate and grid pattern, GAP computes the S-parameters of the grid. However, GAP can only deal with simple planar structures (Fig. 2.4). For a complicated structure, e.g. a grid with holes in the substrate, which will be used in Chapter 3 and Chapter 4, a CAD software application HFSS is applied in this research instead of GAP.

Before HFSS is used in the design, the HFSS simulation result is verified by comparing it with GAP. Figure 2.4 shows a unit cell grid with dipole-dipole configuration for a C-band grid oscillator [3]. The grid is backed by a Rogers RT/*Duroid* 6010 (6.35 mm, $\varepsilon_r = 10.2$) and a mirror.

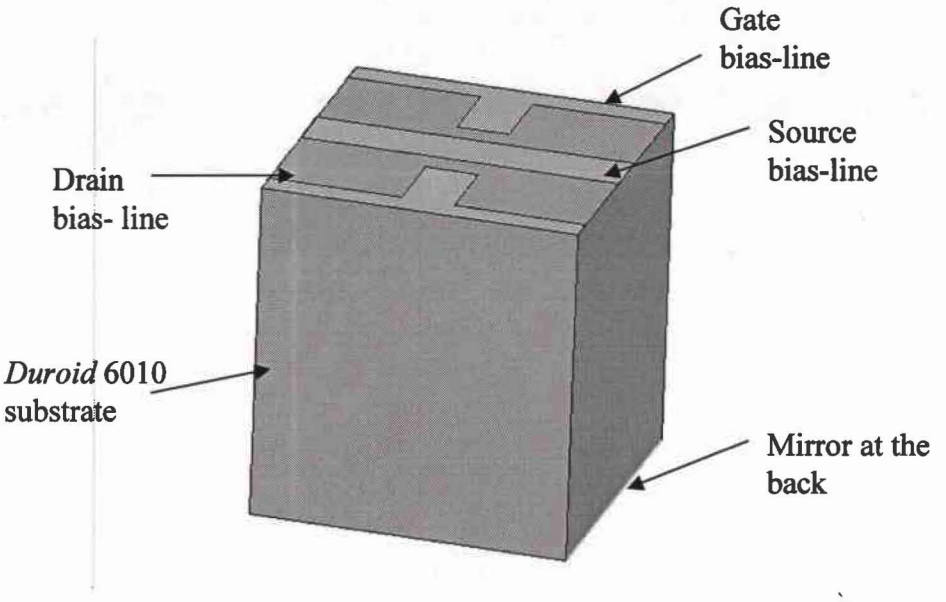


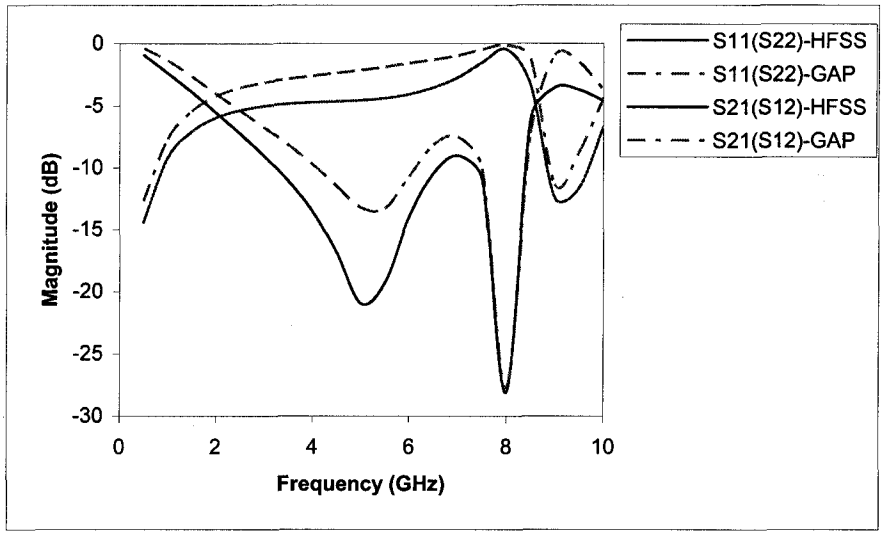
Fig. 2.4 The geometry of a unit cell grid for a C-band grid oscillator. The unit cell has a dimension of 6 mm × 6 mm. The width for the metal grid lines is 1 mm.

The active device for this grid oscillator is an HP-Avantek ATF-26836 MESFET transistor. The oscillation for this grid oscillator was observed at 2.7 GHz and 6.4 GHz [6].

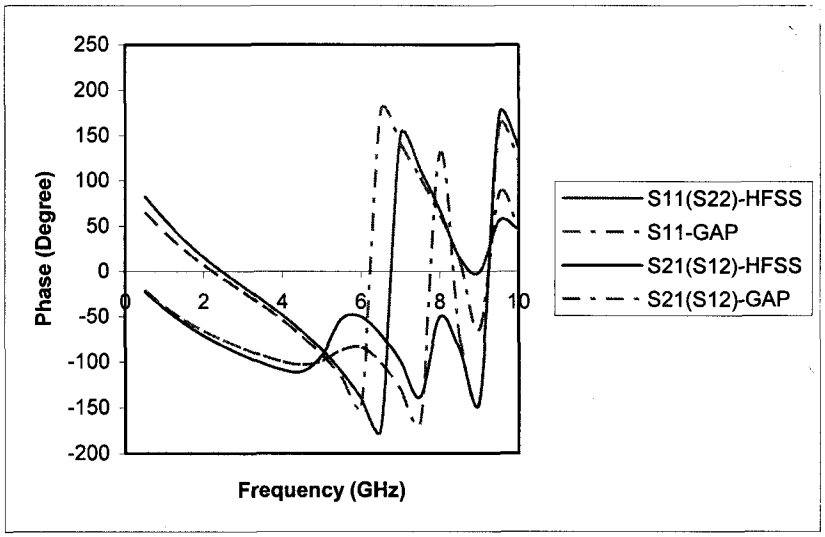
Figure 2.5 compares the simulated S-parameters between HFSS and GAP. Both simulation results have the similar tendency for the magnitude and phase. They have fair correlation except the middle range of frequencies being simulated, which might be caused by the selection of the mesh size during the simulation.

The circular function was simulated by a CAD software called Advanced Design System (ADS) with the small signal S-parameters of the transistor (V_{ds} = 1.5 V, I_{ds} = 10 mA) and the simulated S-parameters of the grid, either by GAP or by HFSS. Figure 2.6 (a) and (b) are the circular functions obtained by using HFSS and GAP results, respectively. Although S-parameters obtained from HFSS are different from GAP, both circular functions using these results predict similar oscillation frequencies which are also close to the measurement report in reference [6].

Therefore, the circular function comparison results indicate the new CAD software – HFSS is trustworthy.

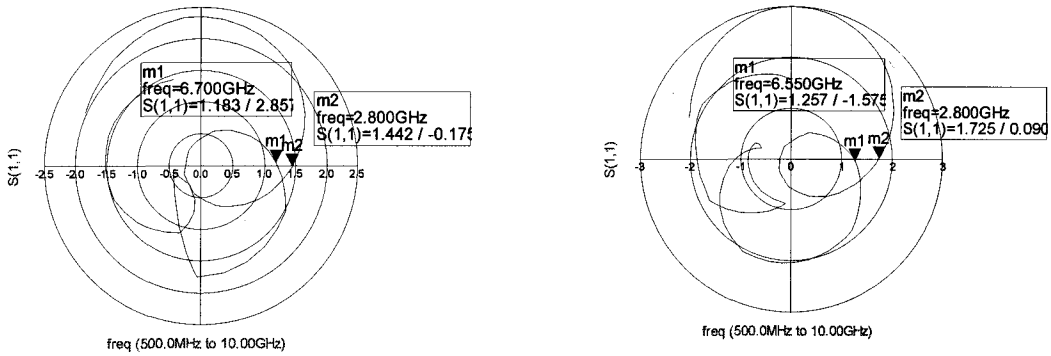


(a)



(b)

Fig. 2.5 The comparison of S-parameters simulated by HFSS and GAP for the unit cell grid in Fig. 2.4. (a) Magnitude of S-parameters, (b) Phase of S-parameters.



(a) (b)

Fig. 2.6 The comparison of circular functions obtained by using S-parameters simulated by HFSS and GAP. (a) Predicted oscillation at 2.8 GHz and 6.7 GHz by using HFSS results, (b) Predicted oscillation at 2.8 GHz and 6.5 GHz by using GAP results.

2.4 Summary

This chapter reviewed the analysis method of grid oscillators. The unit cell approximation was discussed first, followed by the two-port network feedback-oscillator model, in which the passive grid and the active device in each unit cell are represented by a two-port network with a set of S-parameters respectively. The oscillation condition for this circuit model was obtained by the circular function method, i.e., $|C| > 1$ and $\angle C = 0°$ for oscillation starting, and $C = 1\angle 0°$ for steady-state at the respected oscillation frequency. Finally, the simulation result of HFSS was verified validate by comparing with GAP.

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Chapter 3 C-Band Hybrid Grid Oscillator

To study edge effects and impacts of holes in substrates on grid oscillators, a C-band hybrid grid oscillator was designed, fabricated and tested.

Section 3.1 discusses the design and fabrication of a 6×6 C-band grid oscillator using Agilent ATF-36077 HEMT transistors printed on 2.54-mm Rogers RT/*Duroid* with ε_r = 10.2. Section 3.2 presents the experimental results of this grid oscillator.

3.1 Design and Fabrication

The grid oscillator consists of a 6×6 mm^2 unit cell, printed on 2.54-mm-thick Rogers RT/*Duroid* substrate with ε_r =10.2. In contrast to conventional hybrid grid oscillators, in which transistors face up (Fig. 3.1 (a)), this grid oscillator has a hole through the substrate in each unit cell, through which the transistor is embedded in the substrate (Fig. 3.1 (b)). This design is based on the grid oscillator project performed by the Active Antenna Group within the University of Hawaii's CubeSat team [1], who proposed holes in substrate would hinder the propagation of substrate modes, and hence improve the radiation pattern.

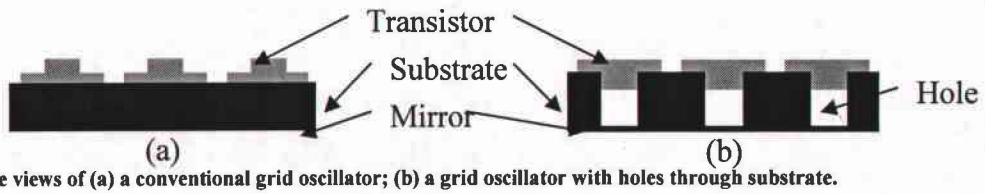
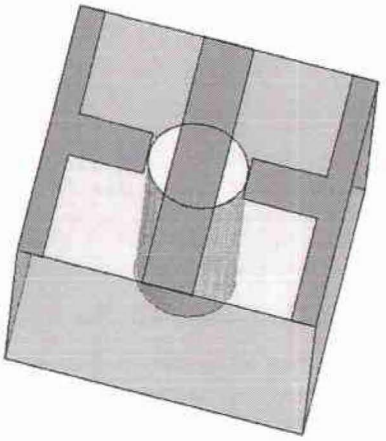


Fig. 3.1 Side views of (a) a conventional grid oscillator; (b) a grid oscillator with holes through substrate.

The unit-cell grid model in HFSS and ADS simulation for this design is shown below in Fig. 3.2. Compared with the simulation result obtained for the grid without holes, the holes in the substrate change little in the oscillation frequency (7%). The fabricated grid oscillator is shown in Fig. 3.3.



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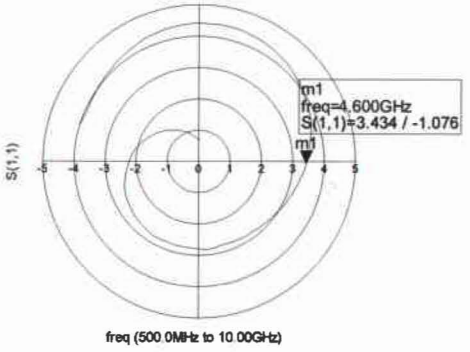

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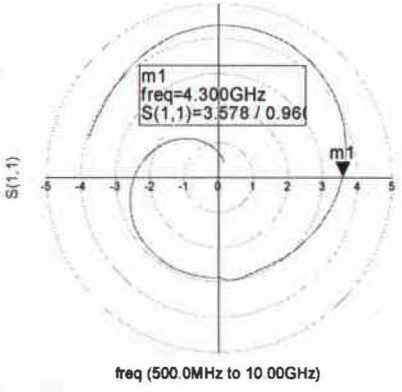


(c)

Fig. 3.2 (a) The unit cell grid design for the C-band grid oscillator, which has dipole-dipole configuration with 1-mm wide metal lines and a hole with 1.78-mm diameter through the substrate, in which the active device is embedded. (b) The grid oscillator is expected to oscillate at 4.6 GHz. (c) The grid oscillator without holes in reference [1] is expected to oscillate at 4.3 GHz.

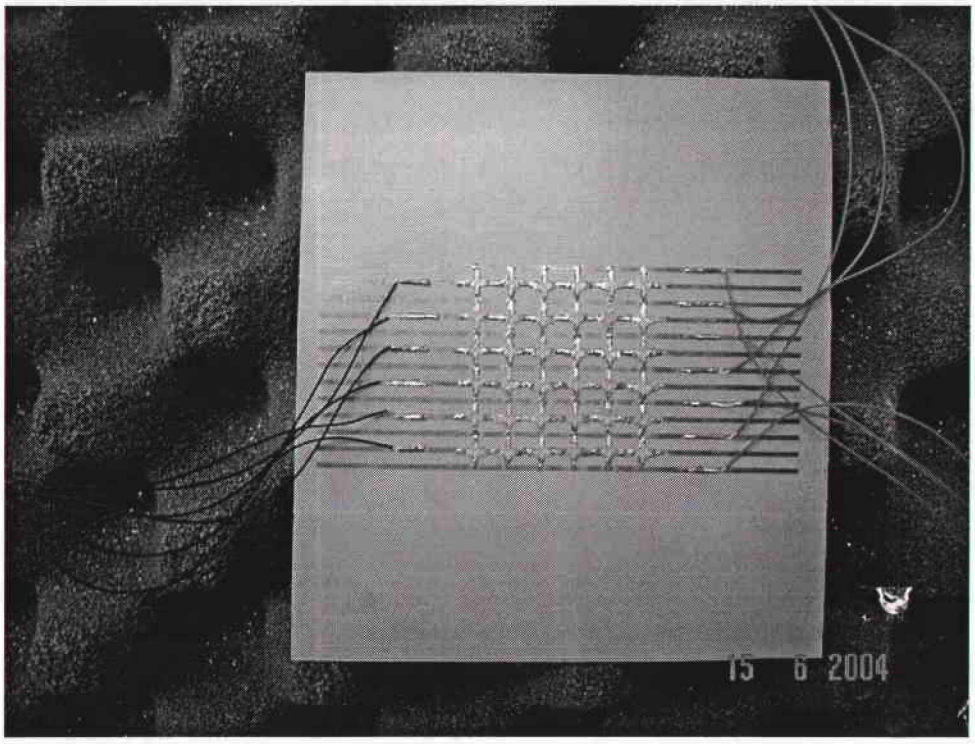


Fig. 3.3 Photograph of the C-band grid oscillator fabricated by Agilent ATF-36077 pHEMT transistors printed on 2.54-mm Rogers RT/*Duroid* with εr = 10.2.

3.2 Experimental Results and Discussion

The experiment setup is shown in Fig. 3.4. An AEL H-1498 horn antenna was used to receive the signal transmitted from the grid oscillator. The range of this antenna is from 2 GHz to 18 GHz. Measurements were taken from a distance R = 1.43 m, found by the far field approximation $R = \frac{2L^2}{\lambda}$, where L is the largest dimension of the grid.

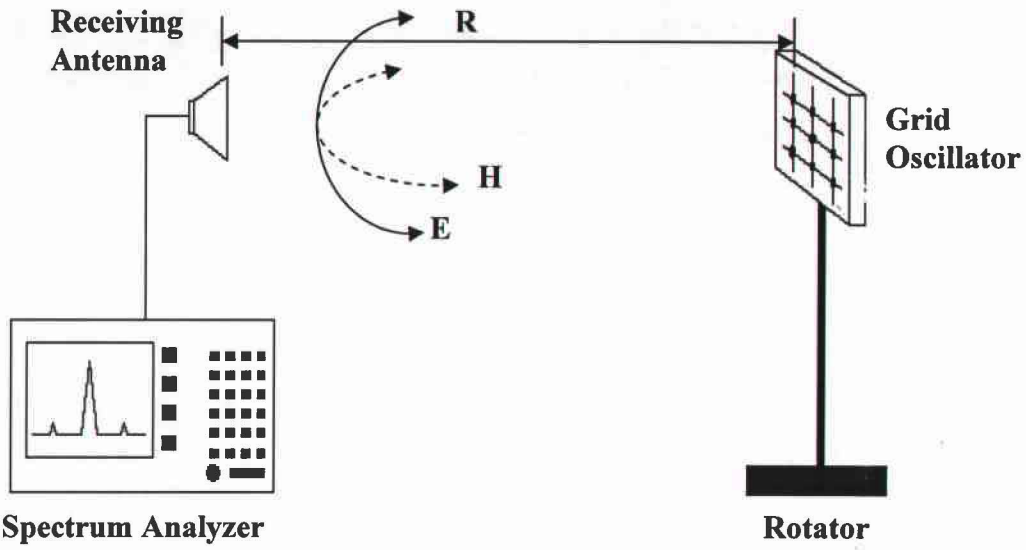


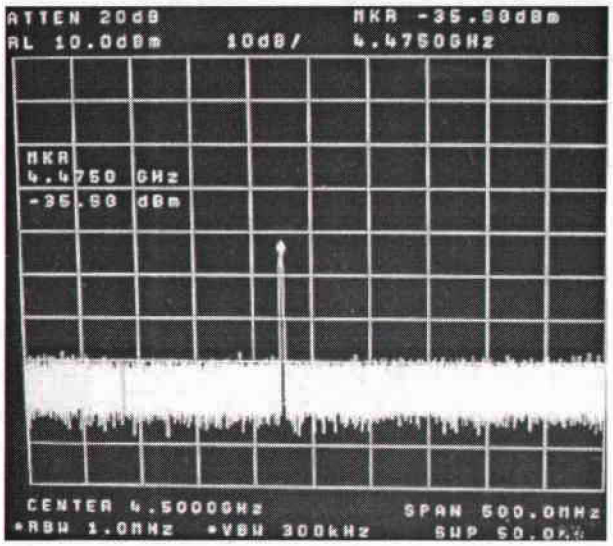
Fig. 3.4 Experimental setup for the measurement of oscillation and radiation pattern.

When the grid was placed and the transistors were biased at Vds = 1.4849 V, Ids = 14.7 mA, Vgs = -0.892 V, Igs = 0.861 mA, a signal of 4.48 GHz was measured on the HP 8564E Spectrum Analyzer, as shown in Fig. 3.5 (a), which is 2.63% lower than the expected 4.6 GHz. The effective isotropic radiated power (EIRP) is 3.48 mW, obtained by using the following equation:

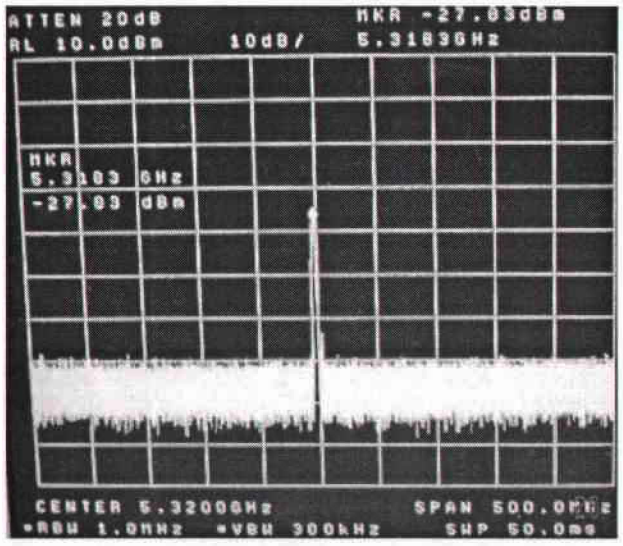
$$EIRP = \frac{P_r}{G_r}(\frac{4\pi R}{\lambda})^2$$

where P_r and G_r are the received power and gain of the horn antenna, respectively.

It is interesting to find that by adjusting the DC bias to Vds = 1.4536 V, Ids = 22.61 mA, Vgs = 1.004 V, Igs = 0.372 mA, a second oscillation mode appears at 5.32 GHz. This one was not predicted by the simulation. The corresponding EIRP is 17.9 mW.



(a)



(b)

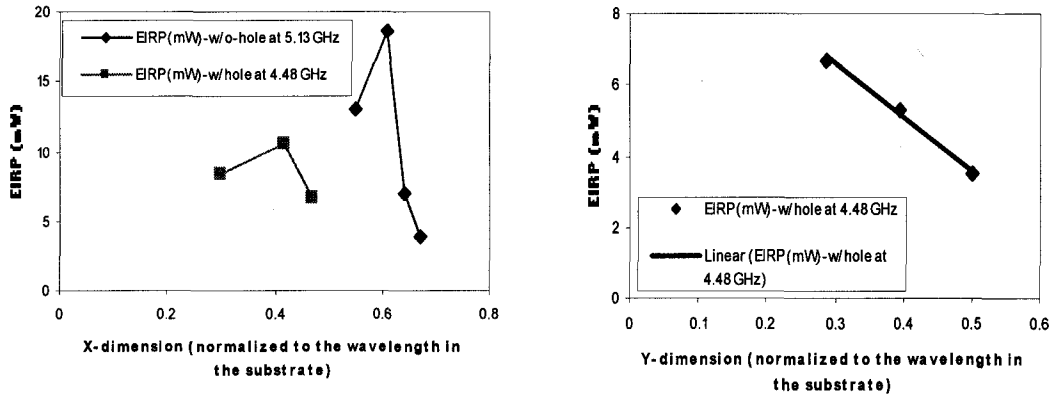
Fig. 3.5 Spectrum for the 6 × 6 C-band grid oscillator: (a) 4.48 GHz at the bias of Vds = 1.4849 V, Ids = 14.7 mA, Vgs = -0.892 V, Igs = 0.861 mA; (b) 5.32 GHz at the bias of Vds = 1.4536 V, Ids = 22.61 mA, Vgs = -1.004 V, Igs = 0.372 mA .

The CubeSat team [1] showed that the total substrate dimensions have an effect on the oscillation frequency and EIRP of the grid oscillator. To investigate if the unpredicted oscillation is due to the edge effect, the edge of the grid oscillator was cut incrementally according to CubeSat team. For each new dimension, the oscillation performance was observed and the EIRP was calculated. The result is shown in Table 3.1. It does indicate the edge effect of the grid oscillator has influence on the oscillation frequency, EIRP, and DC-RF conversion efficiency.

Table 3.1 Comparison of oscillation frequency, EIRP and DC-RF conversion efficiency at different substrate dimensions.

X (cm)	Y (cm)	Frequency (GHz)	EIRP (mW)	DC-RF conversion efficiency (%)
9.8	10.5	4.48	3.48	1.31
		5.32	17.9	4.4
9.8	8.3	4.48	5.32	N/A
9.8	6.0	4.48	6.70	N/A
8.8	6.0	4.48	10.61	7.29
6.3	6.0	4.42	8.43	N/A
		5.72	11.6	4.92

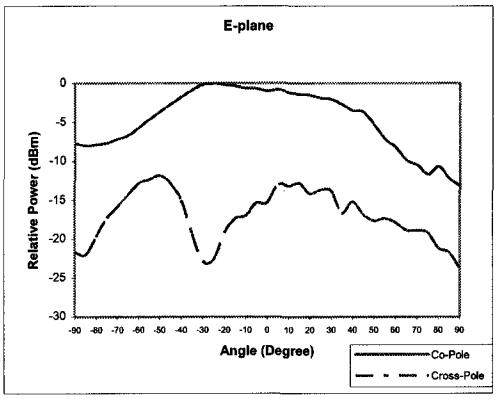
To further investigate the relationship between substrates dimensions and the EIRP, Fig. 3.6 plots the EIRP vs. x- and y-dimensions, respectively. Figure 3.6 (a) compares the EIRP of the grid oscillator with holes and the grid oscillator without holes reported in reference [1] at different x-dimensions. Although the two grid oscillators have different oscillation frequencies, the varying of EIRP with x-dimensions demonstrates similar trend – as the x-dimension increases, the EIRP increases first, and then decreases. In Fig. 3.6 (b), however, the EIRP shows linear decreasing as the y-dimension increases.



(a) (b)

Fig 3.6 EIRP vs. substrate dimensions. (a) Comparison between the grid oscillator with holes and without holes in the substrate. (b) EIRP of the grid oscillator with holes varies with the y-dimension.

The radiation patterns were measured in both the E- and H-planes. Figure 3.4 shows that the E-plane is the plane parallel to the dipoles of the grid, and the H-plane is perpendicular to the dipoles. Figure 3.7 shows the measured E-plane and H-plane radiation patterns for the oscillation frequency at 5.32 GHz, 4.48 GHz, and 5.72 GHz. The radiation patterns did not show significant improvement as the CubeSat team had hoped.



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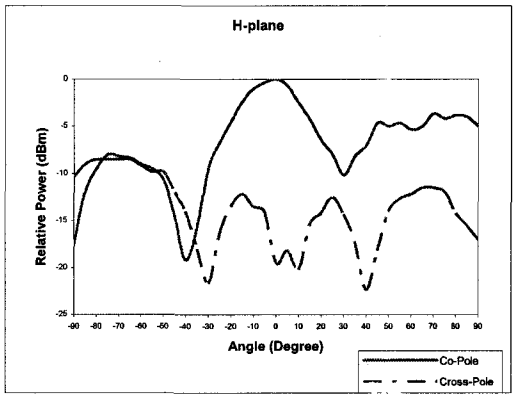
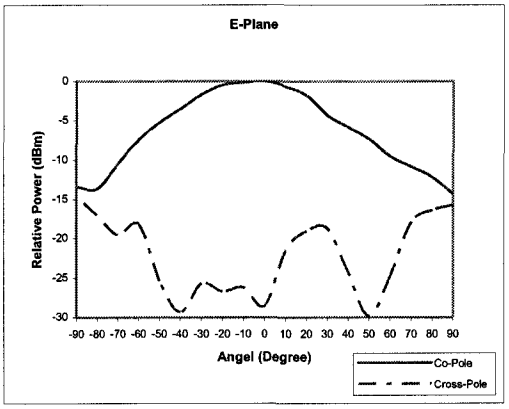


(a)-2



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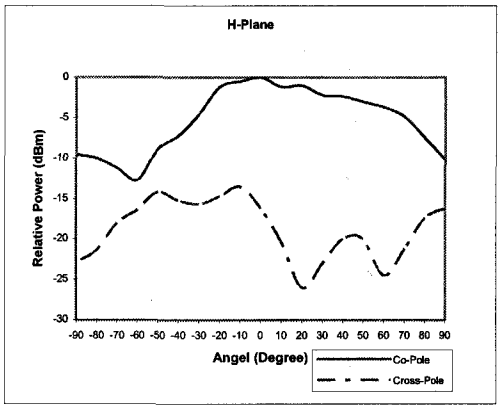

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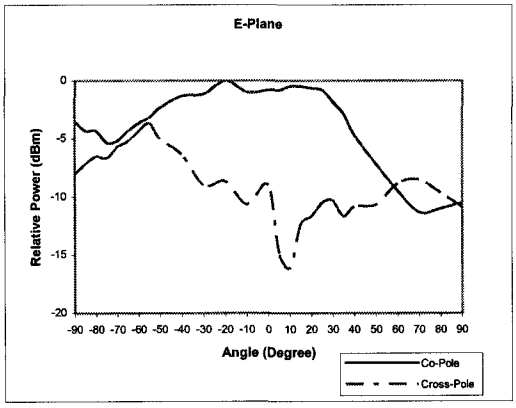

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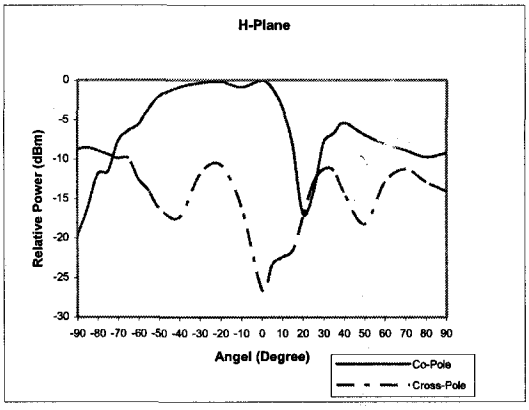


(c)-2

Fig. 3.7 Measured radiation pattern for the C-band grid oscillator. (a) x = 9.8 cm, y = 10.5 cm, and oscillation at 5.32 GHz; (b) x = 8.8 cm, y = 6.0 cm, and oscillation at 4.48 GHz; (c) x = 6.3 cm, y = 6.0 cm, and oscillation at 5.72 GHz. -1. E-plane, -2 H-plane.

3.3 Summary

This chapter presented a Section 6×6 C-band grid oscillator fabricated with Agilent ATF-36077 pHEMT transistors printed on 2.54-mm Rogers RT/*Duroid* with ε_r = 10.2. The experimental results showed a 4.48 GHz oscillation, which is within 3% of the simulation result, but the edge effect caused a second oscillation mode at 5.32 GHz and 5.72 GHz, when the substrate dimensions was varied. The edge effect also had an impact on EIRP.

References

[1] T. Fujishige, A. Ohta, and M. Tamamoto, "Active antenna for UH CubeSat," EE 496 project report, Department of Electrical Engineering, University of Hawaii at Manoa, 2002.

Chapter 4 MMIC AlSb/InAs HEMT Grid Oscillator

This chapter presents the design of MMIC AlSb/InAs HEMT grid oscillators. Section 4.1 summarizes the characteristics of a new high-frequency solid-state device – the AlSb/InAs HEMT. Section 4.2 presents the design of a 50-GHz (Q-band) MMIC AlSb/InAs HEMT grid oscillator. Section 4.2 and 4.3 discuss two power issues: the optimum power operating point by large signal S-parameters and the reduction of substrate mode power by adjusting the unit cell dimensions, respectively. Section 4.4 discusses the experimental results of the fabricated MMIC oscillator and the device failure.

4.1 Characteristics of AlSb/InAs

4.1.1 Overview of HEMTs

High electron mobility transistors (HEMTs) [1] are very important and mature electronic III-V semiconductor devices. Compared to conventional metal semiconductor field-effect transistors (MESFETs), they have enhanced electron mobility due to the heterojunction formed between semiconductors of different bandgaps, e.g., GaAs/AlGaAs or InGaAs/InP, which are lattice matched to each other either exactly or pseudomorphically.

Figure 4.1 shows the band diagram of a basic HEMT structure. In a HEMT, the large bandgap material is usually highly doped, while the small bandgap material is more lightly doped or even intrinsic. To achieve thermal equilibrium, electrons from the wide bandgap material flow into the small band gap material, forming an

accumulation layer of electrons in the potential well adjacent to the interface, which is called a 2-dimensional electron gas (2-DEG). The electrons in the potential well are physically separated from the ionized impurities so that the electron mobility can be drastically enhanced by reducing coulombic ionized impurity scattering.

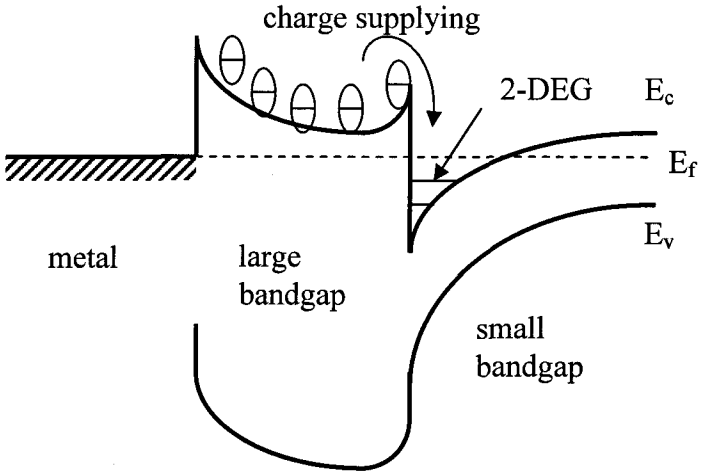


Fig. 4.1 Band diagram of a basic HEMT structure.

The improved electron mobility leads to high drain current, and thus high transconductance at the same amount of charge modulation, so that this device shows excellent high-frequency characteristics and offers potential advantages in microwave, millimeter-wave, and high-speed digital integrated applications.

4.1.2 AlSb/InAs HEMT

AlSb/InAs HEMTs are recently developed III-V material semiconductor devices. Compared to those of current state-of-the-art $In_xGa_{1-x}As$-channel HEMTs, they have higher electron mobilities and velocities due to the property of InAs [2]-[8].

Therefore, they have intrinsic advantages for next generation low-noise, low-dc power and high-frequency electronic circuits in applications that require light-weight power supplies, long battery lifetimes, improved efficiency and high component density.

Compared to the key material used in high performance FETs, i.e., InP, GaAs, and $In_{0.53}Ga_{0.47}As$, InAs has properties of smaller electron effective mass and larger Γ-L valley separation, as shown in Table 4.1, which result in higher electron mobility and higher electron peak velocity [3].

Compared to $In_xGa_{1-x}As$-channel HEMTs, the considerably larger conduction band discontinuity (1.35 eV) of the AlSb/InAs heterojunction enables the formation of a deeper quantum well with the associated benefits of a larger 2-dimensional electron gas (2-DEG) sheet charge density, superior carrier confinement and improved modulation efficiency [3].

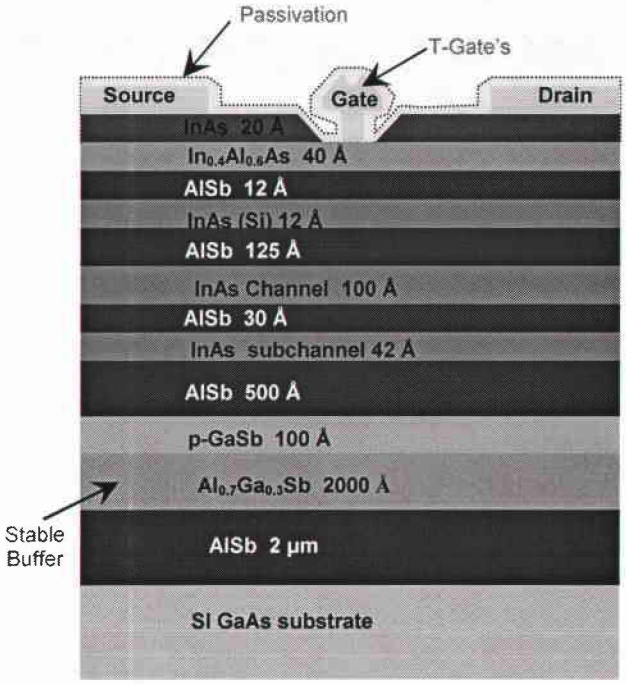
Table 4.1 Properties of key materials used in FET channel [3]

	InAs	$In_{0.53}Ga_{0.47}As$	GaAs	InP
Electron effective mass (m_Γ^*/m_0)	0.023	0.041	0.067	0.077
Electron mobility (cm^2/V-sec@300K, $N_D=10^{17}cm^{-3}$)	16000	7800	4600	2800
Γ-L valley separation (eV)	0.9	0.55	0.31	0.53
Electron peak velocity (10^{17}cm/sec)	4.0	2.7	2.2	2.5
Energy band gap (eV@300K)	0.36	0.72	1.42	1.35

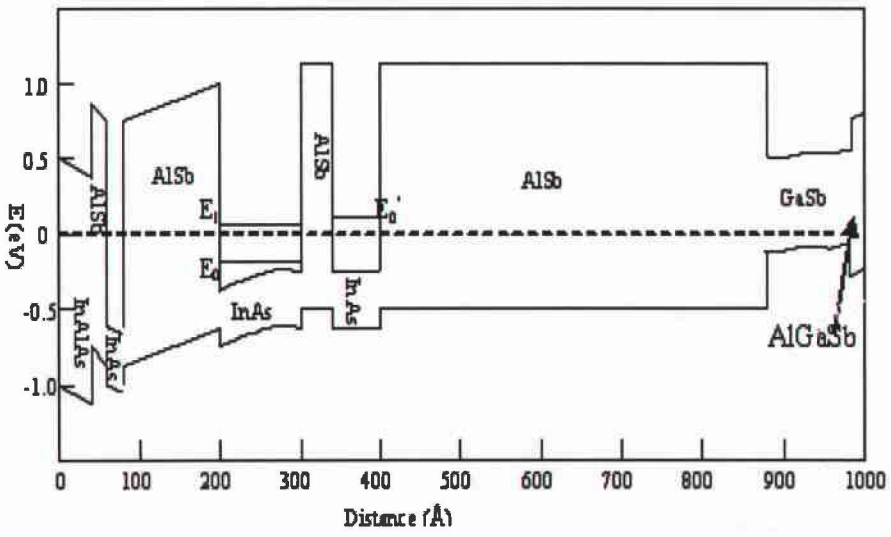
Though AlSb/InAs HEMTs have the intrinsic material advantages, the small bandgap of InAs also results in large gate leakage current, high output admittance, and trapping effects due to holes generated by impact ionization. To fully exploit the advantages of the intrinsic material properties and realize the performance potential, the device structure has to be designed to reduce those negative effects.

Figure 4.2 illustrates the structure of an AlSb/InAs HEMT compatible with standard monolithic-milimeterwave-integrated-circuit (MMIC) processes at Northrop Grumman Space Technology (NGST).

The 2.0 μm AlSb buffer layer accommodates the lattice mismatch between the HEMT material and the GaAs substrate. A Si-doped thin InAs layer located adjacent to the AlSb barrier is used to increase the sheet charge [5]. A thin undoped InAs sub-channel is introduced to reduce impact ionization effects due to its narrow bandgap, which may increase the gate leakage current in the device [2], [3], [6]. The use of the $In_{0.4}Al_{0.6}As$/AlSb composite barrier above the InAs quantum well enhances the insulating property and enables a gate recess process to be employed [3], [6]. A Si-doped p-GaSb layer is intended to drain a portion of impact ionization-generated holes back to the source contact rather than having them remain in the AlSb buffer layer where they are likely to cause trapping effects or be collected at the gate contact and thereby increase the gate leakage current [2], [3], [6]. An insert of $Al_{0.7}Ga_{0.3}Sb$ on the AlSb buffer enables a shallow mesa isolation and makes the device formation completely compatible with standard MMIC processes at NGST [2].



(a)



(b)

Fig. 4.2 (a) Cross-section of AlSb/InAs HEMTs [2]. (b) Energy band diagram of the structure in (a) [3], [6].

For a HEMT with 0.15 μm Pt/Au T-gate fabricated at NGST with structure shown in Fig. 4.2, a peak transconductance of 600 mS/mm with a drain bias of 0.5 V and a drain current of 120 mA/mm has been achieved [2]. Figure 4.3 shows the drain current vs. drain voltage and gate voltage. Figure 4.4 shows the RF performance for an InAs HEMT with two fingers and an 80-μm wide gate. The device obtained an extrinsic f_T of 110 GHz, and f_{max} of 105 GHz at a drain bias of 0.5 V and drain current of 12 mA. By fitting equivalent circuit models (Fig. 4.5) to the measured S-parameters, the intrinsic f_T and f_{max} of 135 GHz and 240 GHz is estimated at the V_{ds} = 0.5 V.

From what was described above, the AlSb/InAs HEMT has excellent performance at of high operational frequencies due to its intrinsic material properties and unique structure. This makes it a good candidate for millimeter-wave systems.

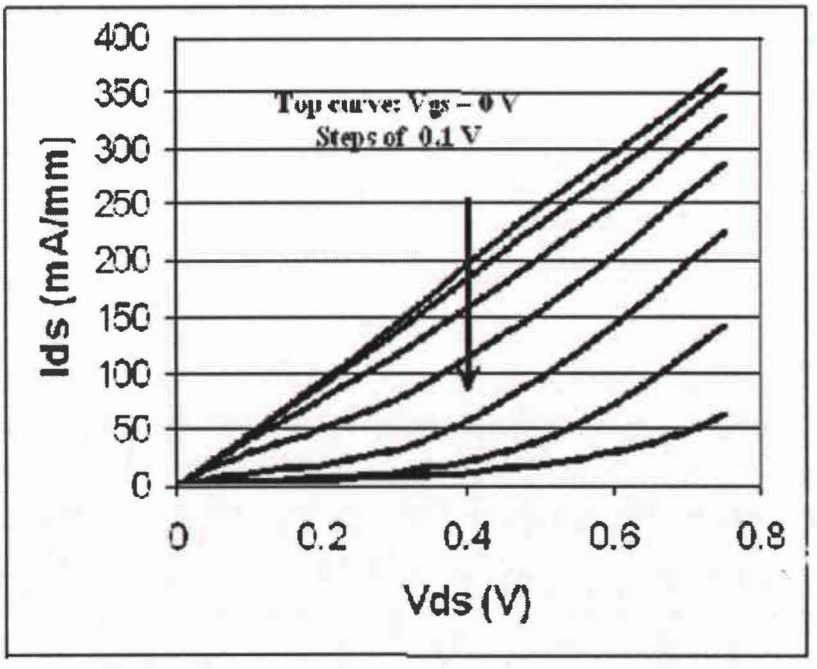


Fig. 4.3 DC characteristics of an AlSb/InAs HEMT with 0.15 μm gate: Ids vs. Vds. at various Vgs [2].

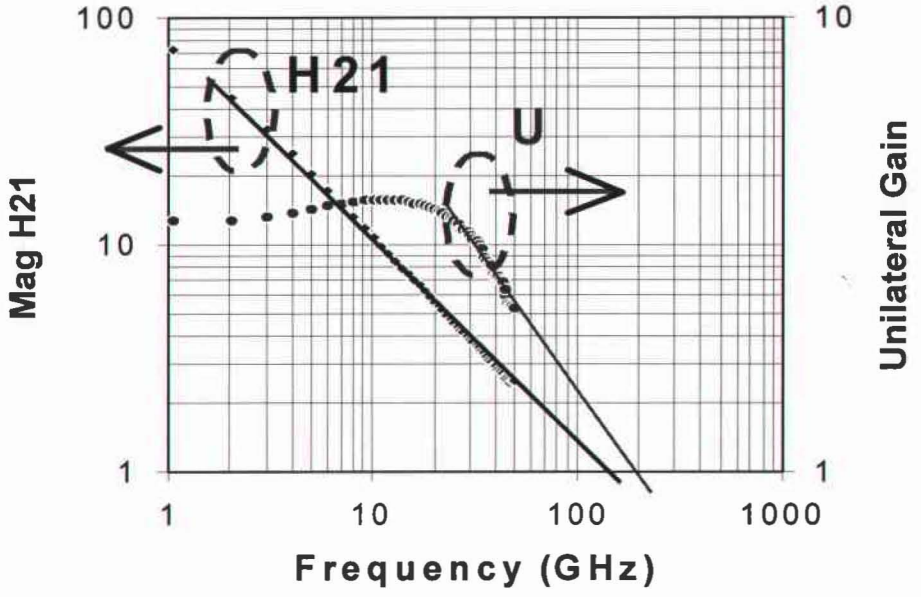


Fig. 4.4 Magnitude of H21 and unilateral gain as a function of frequency for AlSb/InAs HEMT with 0.15 μm and 2 × 40 μm gate biased at Vds = 0.5 V and Ids of 150 mA/mm. Extrapolated extrinsic f_T = 110 GHz and fmax = 105 GHz [2].

Linear Model		
Parameter	Value	Units
Cgs	0.05	pF
Cgd	0.015	pF
Cds	0.0107	pF
Gm	55	mS
Rds	75	Ω
Tau	0.1	pS
Rg	4	Ω
Rs	3	Ω
Rd	4.5	Ω
Ri	10	Ω
Rj	0	Ω
Lg	0.0041	nH
Ls	0.0006	nH
Ld	0.0105	nH

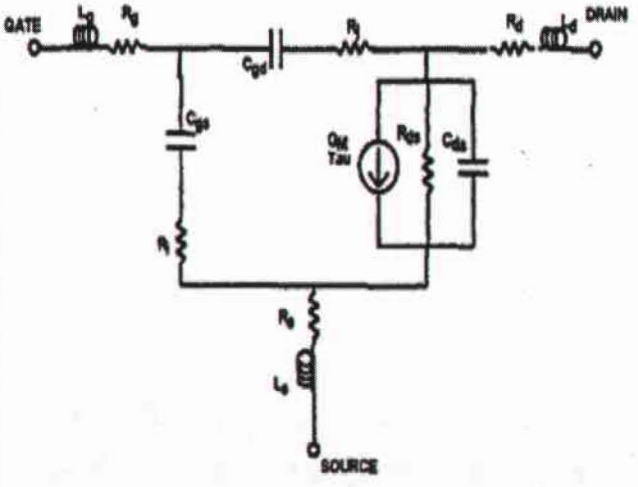


Fig. 4.5 Small-signal equivalent circuit model for AlSb/InAs HEMT with 0.15 μm and 2 × 40 μm gate [2].

4.2 Design of MMIC AlSb/InAs HEMT Grid Oscillator at 50GHz

Compared to the conventional HEMTs based on GaAs or InP material system, AlSb/InAs HEMTs have the advantages of low noise, low consumed power and high-operational frequency, which makes it more suitable to work with at millimeter-wave range. On the other hand, its low power consumption limits the available output power. Therefore, to meet the requirement of high frequency and available power level, quasi-optical combining techniques can be applied in circuits which employ AlSn/InAs HEMTs.

To test this idea, in this research, the first MMIC grid oscillator using AlSb/InAs HEMTs on a GaAs substrate was designed. Since NGST's GaAs MMIC process was used for the fabrication, two parameters which affect the oscillation of the grid oscillator - dielectric constant ($\varepsilon_r = 12.9$) and thickness (d = 0.10 mm) of the substrate are fixed. Therefore, the model of the HEMTs and geometry of the unit cell have to be selected properly in the design to satisfy the oscillation conditions ($|C| > 1$ and $\angle C = 0°$ for start-up, and $C = 1\angle 0°$ for steady-sate).

In the investigation of Q-band grid oscillator, the dipole-dipole grid configuration was used. Its S-parameters were obtained by HFSS. The device model and unit cell size were varied to get different circular functions, as shown in Table 4.2. The circular function was simulated using ADS installed with NGST's ABCS design kit. As expected, the results of Table 4.1 indicate that for a particular device, the smaller unit cell results in a higher oscillation frequency. Device sdHCA4CKT-ms1_0 with 340 × 340 μm^2 unit cell dimension shows the desired high oscillation frequency of 52 GHz.

Table 4.2 Circular function varied with the active device model and unit cell size for dipole-dipole grid without vias

Device model	Description	Unit cell size (μm)	Oscillation frequency (GHz)	Circular function
sdHCA8CKT-ms1_0	8 finger with gate width of 200 μm	1000	21	5.85
		340	30	1.32
sdHCA4CKT-ms1_0	4 finger with gate width of 100 μm	1000	25.5	3.89
		340	52	2.58

In the design of a MMIC grid oscillator with unit-cell size 340 μm, to avoid the potential fabrication problem due to cross-over of different metal layers, grounding vias were used to ground the source of each device. To investigate the impact of the via to the oscillation, HFSS was used to obtain the S-parameters for the feedback network in the unit cell model. Figure 4.6 shows the unit cell designed for 50 GHz oscillation. Figure 4.7 compares the S-parameters of the grid with and without the vias, and indicates that the via affects the S-parameters significantly. Figure 4.8 shows the circular functions of the grid oscillator with expected oscillation at 50 GHz by using via design and 52 GHz without via. There is not much difference in the oscillation frequency for the grid with and without via, but with via the magnitude of the circular function is much smaller than without via.

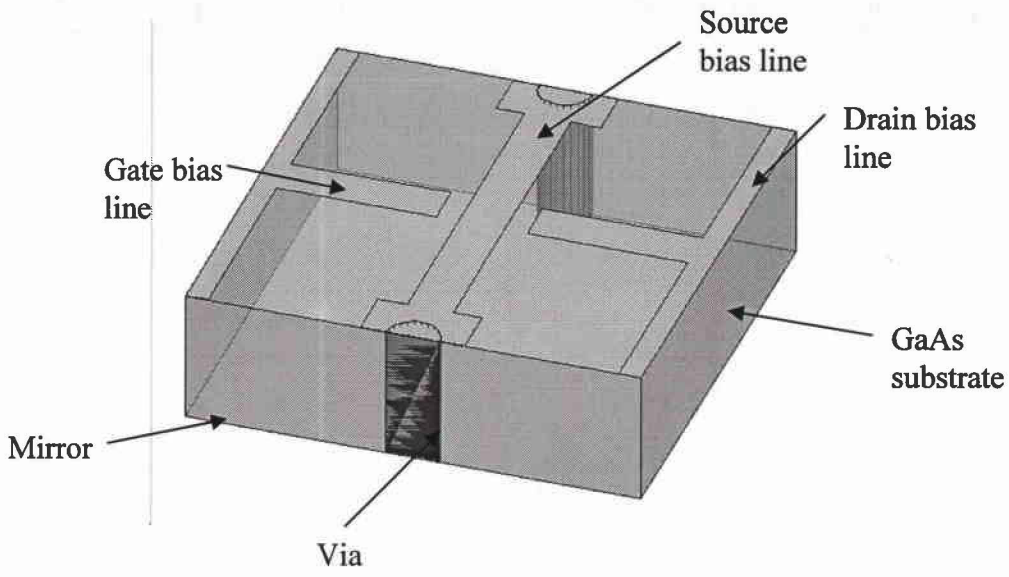
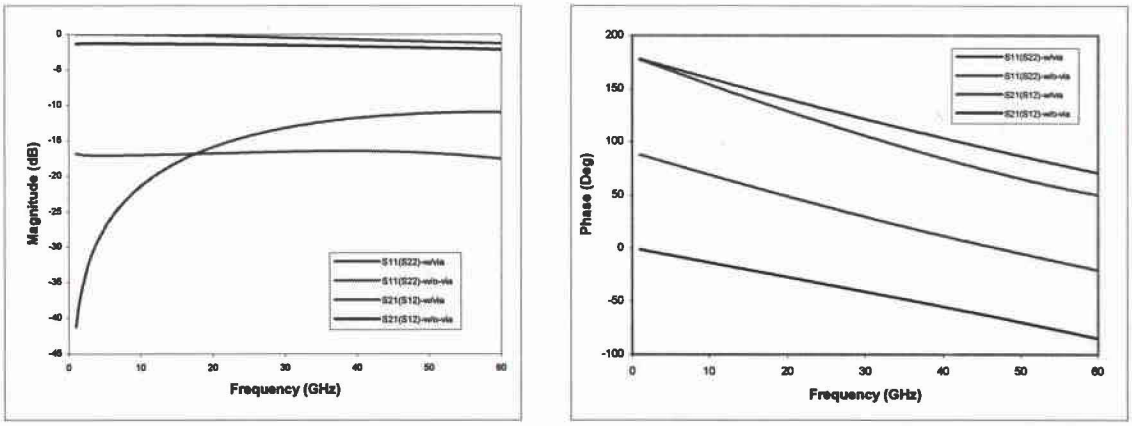
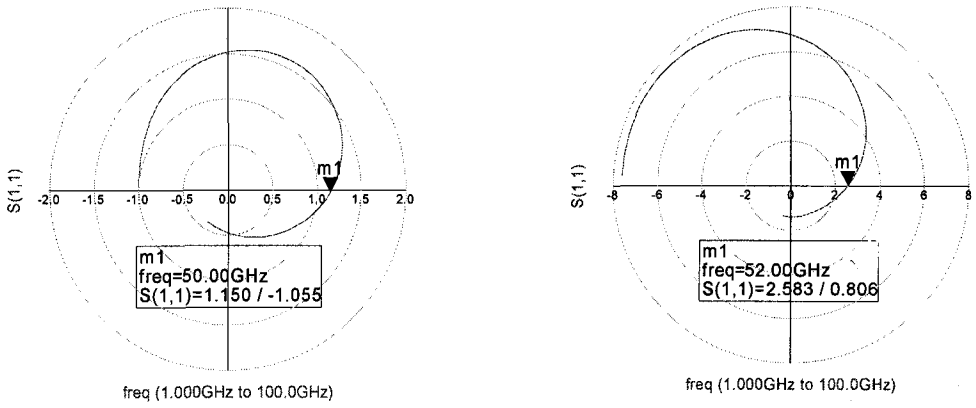


Fig. 4.6 Unit cell geometry of the grid designed at 50 GHz with via at the both sides of the sources.



(a) (b)

Fig. 4.7 Comparison of S-parameters for grid with and without via: (a) magnitude, (b) phase.



(a) (b)

Fig. 4.8 Circular function comparison between the grid design with and without via. (a) The expected oscillation at 50 GHz with via for grounding, (b) the expected oscillation at 52 GHz without via.

4.3 Power Optimization

The circular function used to design the grid oscillator in the previous section is based on the transistor small-signal S-parameters, which predicts if the combination of an active device and grid geometry will make an oscillation possible at some frequency. However, it doesn't give any information about if the grid will yield high or low power. To address this issue, the grid oscillator power optimization theory was presented in [9], in which based on the large-signal S-parameters of the transistor, a feedback network circuit model for the grid was synthesized for the transistor to operate at maximum power-added efficiency. The difference between the corresponding optimum circular function and the circular function of the designed grid oscillator indicates the power-operating point.

4.3.1 Large-Signal S-Parameters and Gain Saturation

In Chapter 2, it was stated that a grid oscillator can be viewed as a transistor connected to a feedback network which contains the load, e.g., free space. If the transistor is considered as an amplifier, then the general feedback amplifier model can be used to study large-signal S-parameters of the transistor and its gain saturation, as shown in Fig. 4.9 (a).

The amplifier adds together the input RF power and the added power (e.g., a fraction of the DC power converted to RF power), and then delivers the output RF power. Therefore, the added power can be expressed by

$$P_{add} = P_{out} - P_{in} \tag{4.1}$$

The oscillator converts a fraction of the input DC power into output RF power. At steady-state, a portion of the output RF power, e.g., oscillator power must be consumed in the load of the feedback network to maintain the power returned to the amplifier input to be P_{in}. The oscillator power, P_{osc}, can be expressed by

$$P_{osc} = P_{out} - P_{in} \tag{4.2}$$

Equations (4.1) and (4.2) indicate that the oscillator power is equal to the added power of the amplifier at the steady-state. Therefore, optimizing the oscillator power is same as optimizing the feedback amplifier added power.

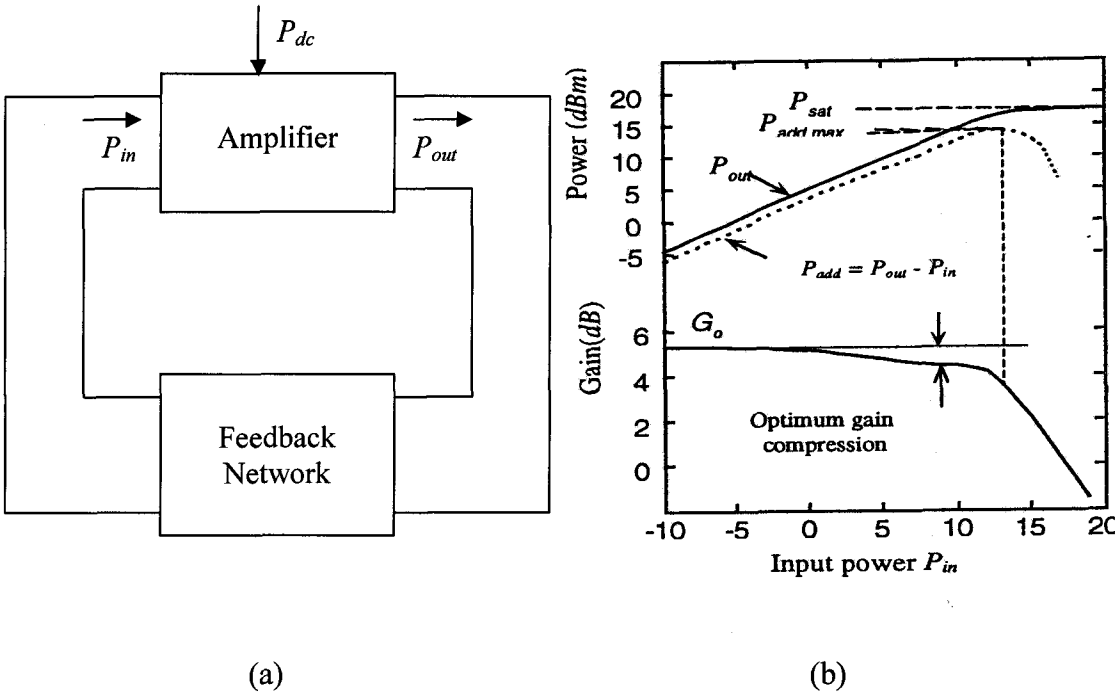


Fig. 4.9 (a) The feedback oscillator topology, and (b) Power- and gain- saturation characteristics for a typical device. [9]

Figure 4.9 (b) illustrates the typical transistor power- and gain-saturation characteristics. At low input power levels, the performance of the transistor is approximately linear, i.e., a linear increase in added power as well as output power with increasing input power. As the input power continue to increase, the increasing pace of the output power and also the added power cannot keep up with the input power and the gain decreases until the output power doesn't increase any more at a certain input power level. This phenomenon is called power saturation. At the point at which the output power saturates, the added power achieves the maximum. This point is called the oscillator power optimization point, or maximum oscillator power point. At this point, the amplifier gain is compressed a certain amount, which corresponds to

the optimum gain compression. After this point, the added power decreases as the input power further increases, and the gain drops dramatically.

At the start-up of the oscillation, the transistor works in the linear region and the circular function evaluated by small-signal S-parameters satisfies $|C| > 1$ at phase 0°. At steady-state, the transistor operates in the nonlinear region, where its small-signal S-parameters are no longer valid. Large-signal S-parameters must be used to evaluate its circular function and satisfy $C = 1 \angle 0°$. Large-signal S-parameters of a transistor can be approximated as proposed by Johnson [10] by reducing the small-signal $|S_{21}|$ while keeping other S-parameters as same as small-signal S-parameters. The large signal $|S_{21}|$ at the maximum oscillator power point can be obtained by the following procedure [9]:

1. At the desired oscillation frequency, calculate the small-signal maximum-efficient gain, $G_{ME,ss}$. The maximum-efficient gain [11], [12] for an oscillator maximizes the difference between output and input power rather than their ratio in the gain definition for amplifier. $G_{ME,ss}$ is defined as

$$G_{ME,ss} = \frac{\left|S_{21}/S_{12}\right|^2 - 1}{2(K\left|S_{21}/S_{12}\right| - 1)} \tag{4.3}$$

   where

$$K = \frac{1 + \left|S_{11}S_{22} - S_{21}S_{12}\right|^2 - \left|S_{11}\right|^2 - \left|S_{22}\right|^2}{2\left|S_{12}\right|\left|S_{21}\right|}$$

2. Calculate the large-signal gain corresponding to maximum added power, $G_{ME,opt}$ by

$$G_{ME,opt} = \frac{G_{ME,ss} - 1}{\ln G_{ME,ss}} \tag{4.4}$$

3. Substitute $G_{ME,opt}$ for $G_{ME,ss}$ in (3.3) and solve for the large-signal $|S_{21}|$.

For a designed grid oscillator at 50 GHz by using AlSb/InAs pHEMT model sdHCA4CKT-ms1_0, a Mathcad program (See Appendix A) shows that $|S_{21}|$ will be reduced by 3.87 dB at the oscillator power optimization point compared with the small signal $|S_{21}|$.

4.3.2 Grid Optimization and Its Equivalent Circuit

As stated in Chapter 2, the passive part of the grid oscillator, i.e. metal grating, substrate, mirror and free space, can be modeled as a two-port embedding network. As expected, the simulated S-parameters for this embedding network showed it is reciprocal. Therefore, a lumped equivalent circuit can be used to represent the passive grid, as shown in Fig. 4.10 (a), in which Y_i is the admittance of the lumped elements. This general model can be further specified in the form shown in Fig. 4.10 (b), where the capacitors C_1 and C_2 model the gate-source and drain-source gaps of the grid individually, and the inductor L and resistor R model the metal inductance, substrate thickness, mirror position and resistance of free space. Replacing the 2-port embedding network with the lumped circuit model, the unit cell of a grid oscillator is represented by a model shown in Fig. 4.11 (a). If the resistor is removed, an equivalent one-port negative-resistance model of the grid oscillator is obtained, as shown in Fig. 4.11 (b). Oscillation start-up requires that the absolute value of the negative resistance be greater than the load resistance.

Fig. 4.10 (a) General lumped equivalent circuit for a two-port network. (b) Typical form of the equivalent circuit for a grid [9].

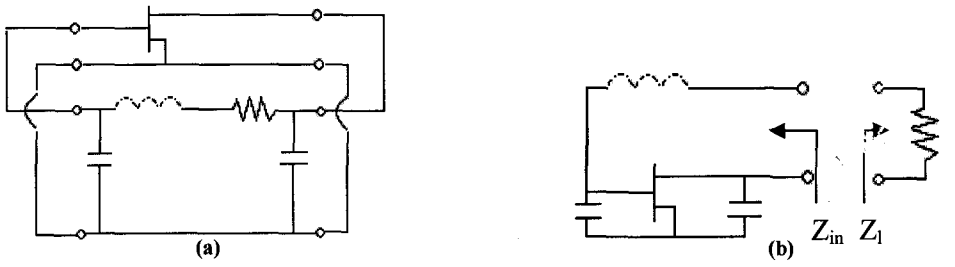


Fig. 4.11 (a) Transistor connected to the equivalent ∏ network. (b) Negative-resistance model of the grid oscillator [9].

By analyzing an oscillator circuit with the lumped embedding element model (see Fig. 4.11), an equivalent circuit for maximum oscillator power can be synthesized as described in [9]. The synthesis procedure is briefly summarized as follows:

1. Obtain large signal-S parameters as described in the previous section for a transistor at the desired oscillation frequency.
2. Convert the approximate large-signal S-parameters to Y-parameters, and calculate the embedding elements by using

$$B_1 = \frac{A_r}{A_i}(C_1 + C_3) + C_2 + C_4 \qquad (4.5\text{-a})$$

$$B_2 = -\frac{1}{A_i}(C_1 + C_3) \qquad (4.5\text{-b})$$

$$B_3 = \frac{1}{|1-A|^2}\left\{(A_r - 1)[C_4 + \frac{A_r}{A_i}(C_1 + C_3)] + A_i C_1\right\} \qquad (4.5\text{-c})$$

$$G_3 = \frac{1}{|1-A|^2}(C_1 + A_r C_3 + A_i C_4) \qquad (4.5\text{-d})$$

where $Y_i = G_i + jB_i$

$C_1 = -\mathrm{Re}(Y_{11} + AY_{12})$ $\qquad$ $C_3 = -\mathrm{Re}(Y_{21} + AY_{22})$

$C_2 = -\mathrm{Im}(Y_{11} + AY_{12})$ $\qquad$ $C_4 = -\mathrm{Im}(Y_{21} + AY_{22})$

and A is the voltage gain ($\frac{V_2}{V_1}$) [13], [14] in the feedback loop as shown in Fig. 4.12, which can be expressed in

$$A = A_r + jA_i$$

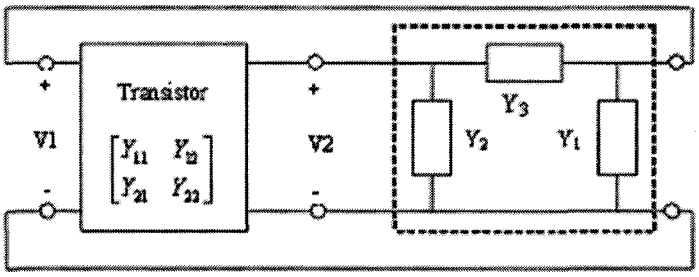


Fig. 4.12 A feedback oscillator consisting of a transistor and a ∏ embedding network.

By using this method, an embedding network is designed to provide the proper feedback for maximum oscillator power, which simultaneously satisfies the oscillation start-up condition evaluated by small-signal S-parameters (|C| > 1) and the steady-state oscillation condition evaluated by large-signal S-parameters (C = 1∠0°). Figure 4.13 shows the optimum lumped equivalent circuit for AlSb/InAs pHEMT

model sdHCA4CKT-ms1_0. Obviously, the two capacitors are not equal. This indicates an asymmetric geometry should be adopted to get the maximum output power.

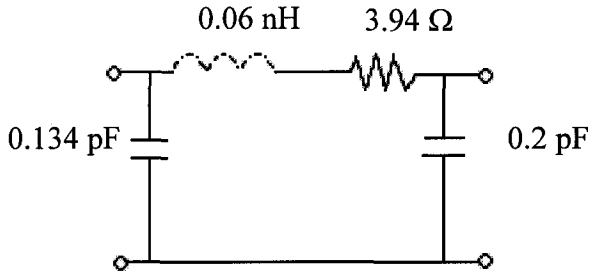


Fig. 4.13 Optimum lumped equivalent circuit for the feedback network of the 50-GHz AlSb/InAs HEMT gunn oscillator.

4.3.3 Optimum Circular Function and Operating Point

Based on the optimum embedding network, the associated small-signal circular function, i.e., optimum circular function, can be computed by using

$$C = \frac{S_{11}S_{11}^{'} + S_{21}S_{12}^{'} - |S||S^{'}|}{1 - S_{12}S_{21}^{'} - S_{22}S_{22}^{'}} \tag{4.6}$$

Comparing the optimum circular function with the designed oscillator's circular function will give one an idea in which region the designed oscillator will operate.

By using the optimum circular function as a benchmark, there are three operation cases related to the power level or gain compression level [9], as shown in Fig. 4.14:

1. Optimum operation. At steady-state, the oscillator works at the maximum oscillator power point, at which its circular function is C_{opt} and its gain compression is

$$GC_{opt} = G_{ME,ss} - G_{ME,opt} \tag{4.7}$$

2. Under-compression (point A). At steady-state, the oscillator works in the high gain region, at which its gain compression GC_A is less than GC_{opt}, and circular function C_A is less than C_{opt} accordingly.
3. Over-compression (point B). At steady-state, the oscillator works in the low gain region, at which its gain compression GC_B is more than GC_{opt}, and circular function C_B is greater than C_{opt} accordingly.

According to the theory of optimum circular function, C_{opt} for the different grid oscillators in Table 4.1 can be calculated. Table 4.2 shows the calculated result, and the comparison to their circular function by using AlSb/InAs HEMT transistor model sdHCA4CKT-ms1_0.

In the designed grid oscillators shown in Table 4.3, the grid with large unit cell size and the grid with small unit cell size but without via have too much feedback. They work at over-compression point B. At this point, the oscillator may suffer from the potential problems such as high harmonic content or degraded device reliability caused by high input power driving large current density at the gate. In contrast, the 340-μm grid with via will work at under-compression point, which is in the near-linear region. Though none of the three designed grid oscillators will work efficiently, the 340-μm grid with via has better efficiency and less potential problems compared to other two. Therefore, this thesis adopted this design. Of course, future work needs to be done to make the grid oscillator work in the region near C_{opt}.

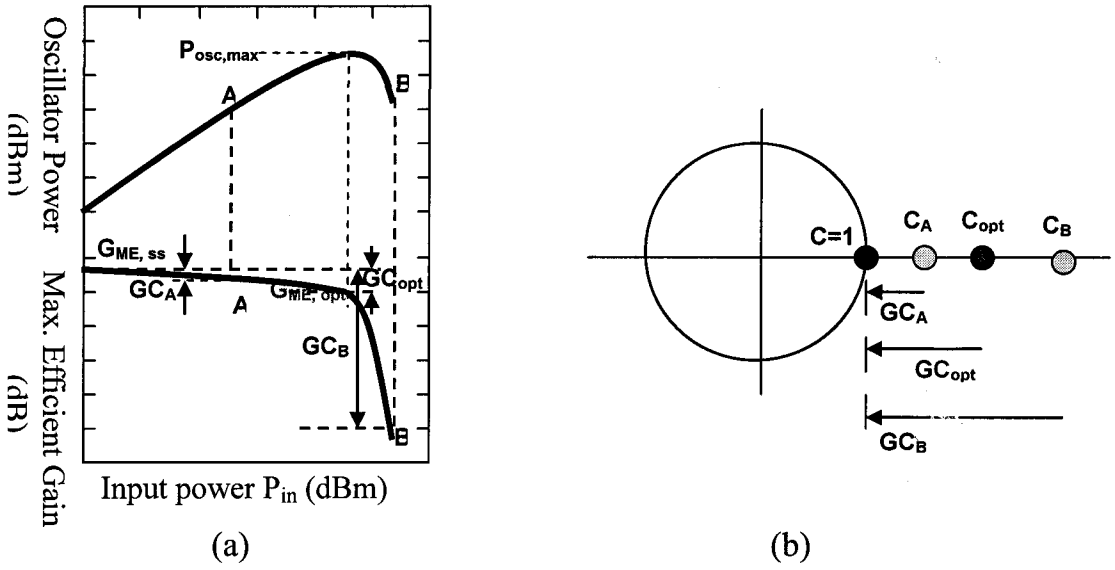


Fig. 4.14 (a) Oscillator operation point: A, B, and optimum; (b) According circular function CA, CB, and Copt for three operating points in (a) [9].

Table 4.3 Comparison of Copt with the circular function for different grid designs.

Device model	Unit cell size (um)	Oscillation frequency (GHz)	Circular function (C)	Optimum $\|C_{opt}\|$	$\frac{\|C_{opt}\|-\|C\|}{\|C\|}\times 100\%$
sdHCA4CKT-ms1_0	1000	25.5	3.89	1.82	-53.2
	340 (w/via)	50	1.152	1.40	21.5
	340 (w/o via)	52	2.583	1.39	-46.2

4.4 Substrate-mode Power Reduction

Grid oscillators are usually mounted on dielectric substrates. Substrates play an important role in the design of grid oscillators. The dielectric constant and thickness of the substrate have great impact on the operation frequency and output power. At high frequencies, the substrate behaves as waveguide for undesired substrate modes which radiate through the edges of the array, resulting poor radiation pattern [15]. More substrate modes are excited as electrical thickness of the dielectric substrate increases, due to the increasing of the frequency or dielectric constant.

Substrate modes affect the radiation pattern, often resulting in undesired high sidelobes. Figure 4.15 [16] shows an example of a poor E-plane pattern for a 36-element HBT monolithic grid mounted on a 740-μm-thick GaAs substrate with a dielectric constant of 12.9 and an operating frequency 34.7 GHz.

To reduce substrate-mode power in grids, one can choose electrically thin substrates [17]. However, this is usually not the case for monolithic grid circuits, since the substrate for monolithic circuits, such as Si (ε_r = 11.9), GaAs (ε_r = 12.9), etc., usually has high a dielectric constant. Therefore, Al-Zayed *et al.* proposed a theory to minimize the effect of substrate modes through a careful choice of unit cell size [18].

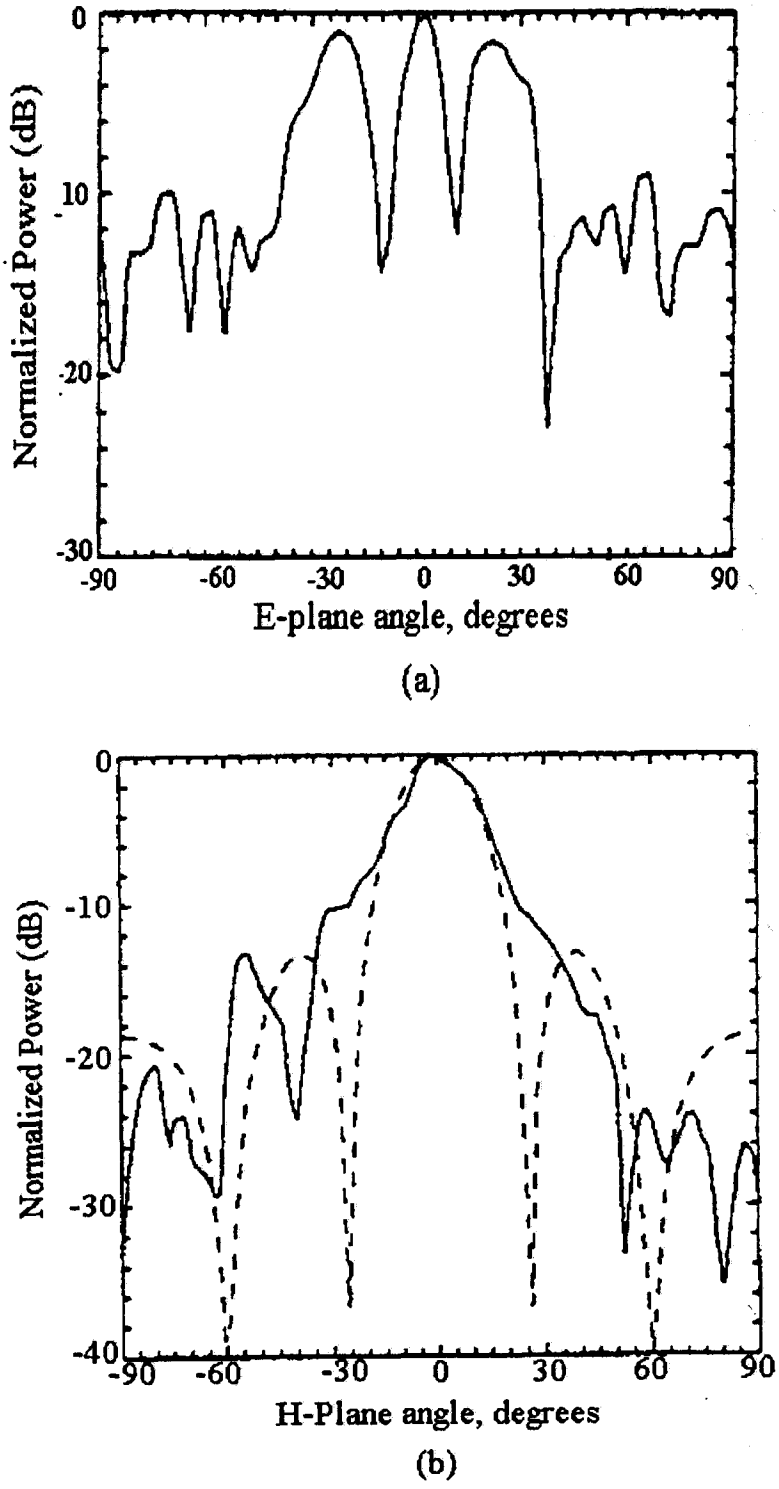


Fig. 4.15 (a) E-plane and (b) H-plane patterns for the 34.7 GHz HBT monolithic grid oscillator [16].

4.4.1 Substrate Modes on a Grounded Dielectric Slab Waveguide

It is known that dielectric substrates are very good waveguides with a fundamental mode that has no cutoff frequency [19], [20]. As shown in Fig. 4.16, a grounded dielectric slab waveguide structure with thickness d can support TM or TE polarization modes, or both.

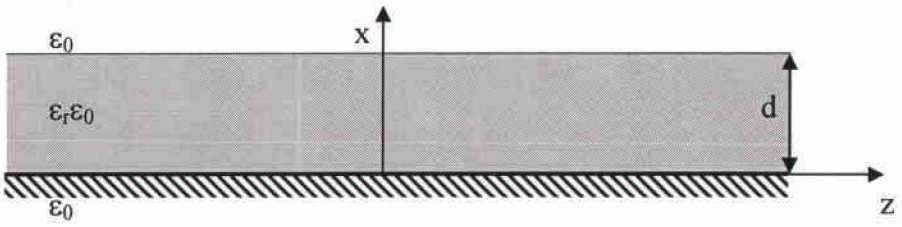


Fig. 4.16 A grounded dielectric slab structure.

To investigate the properties of the guided substrate modes in this structure, such as how many guided modes exist in it, what polarization these modes have, and what their cutoff frequencies are, etc., a set of simultaneous transcendental equations or dispersion relations have to be used [21]-[23].

For TM modes:

$$h\tan(hd) = \varepsilon_r p \qquad (4.8\text{-a})$$

$$h^2 + p^2 = (\varepsilon_r - 1)k_0^{\,2} \qquad (4.8\text{-b})$$

For TE modes:

$$-h\cot(hd) = p \qquad (4.9\text{-a})$$

$$h^2 + p^2 = (\sqrt{\varepsilon_r - 1}k_0)^2 \qquad (4.9\text{-b})$$

where h and p are the cutoff wavenumbers in region $0 \le x \le d$ and $x \ge d$, respectively, and k_0 is the propagation constant in free space.

Equations (4.8) and (4.9) can be solved for cutoff wavenumbers p and h graphically. The intersection of a circle with center point at (0, 0) and radius of $V=\sqrt{\varepsilon_r - 1}k_0 d$ (normalized frequency) and a tangent function curve in the pd vs. hd plane, implies a solution to equation (4.8) and (4.9).

Multiple intersections indicate that more than one TM mode can propagate in the dielectric slab waveguide. Also note that the larger radius $\sqrt{\varepsilon_r - 1}k_0 d$, the more intersections would be obtained. This means that the higher the dielectric constant ε_r, the thicker the dielectric substrate d, or the higher operation frequency, the more modes will exist in a given dielectric substrate.

As an example, Fig. 4.17 is the graphical representation of the dispersion relations for a grounded GaAs slab with dielectric constant ε_r = 12.9 and thickness d = 0.1 mm, which is the case for the substrate for a grid oscillator designed at 50 GHz (Appendix B). It shows that for such a GaAs substrate, only the TM_0 mode can exist.

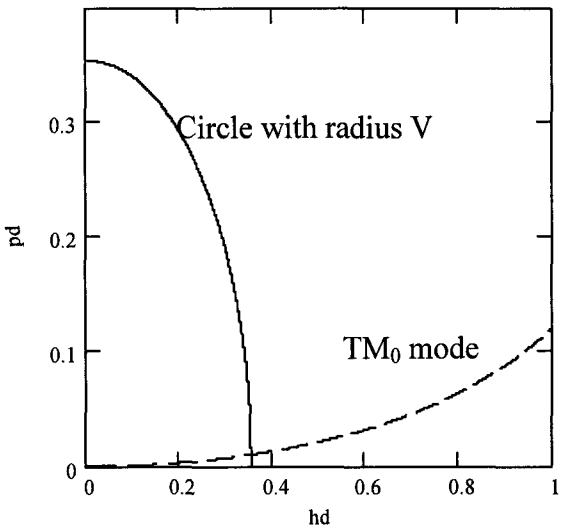


Fig. 4.17 Graphical solution of the dispersion relations for the modes that exist in a grounded substrate with εr = 12.9 and d = 0.1 mm at 50 GHz.

4.4.2 Substrate Mode Power

To find how the substrate mode existing in the substrate impacts the radiation pattern of the grid oscillator, consider an array of short dipoles on a substrate, as shown in Fig. 4.18.

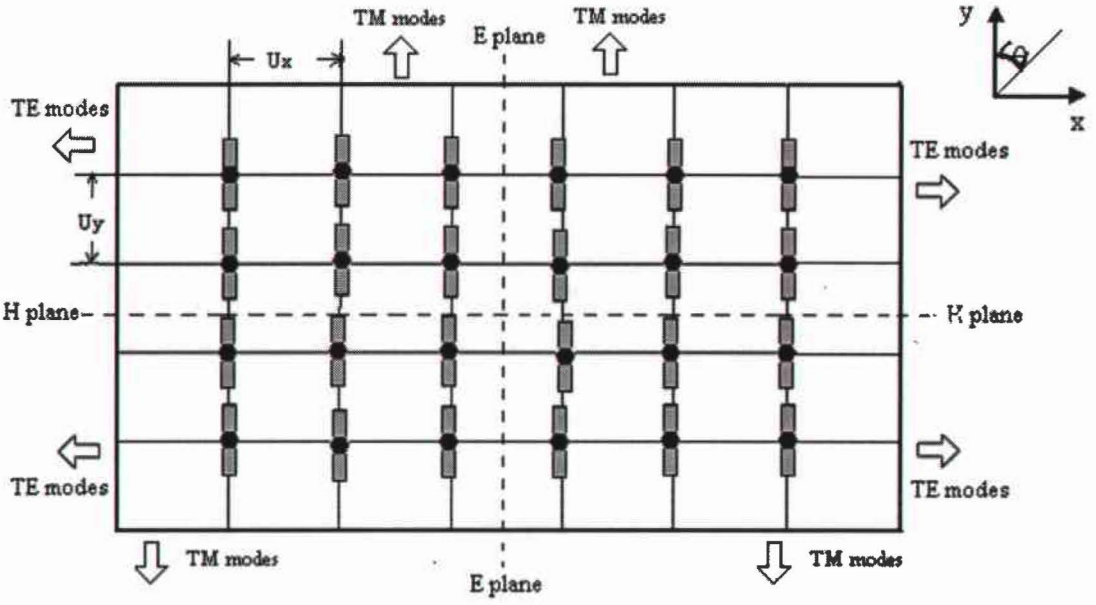


Fig. 4.18 Geometry of an M × N two dimensional planar array.

The substrate-mode pattern for a dipole antenna printed on a dielectric substrate is such that TE substrate modes propagate perpendicular to the dipole axis, and TM substrate modes propagate parallel to the dipole axis (Fig. 4.18) [24]. Therefore, these TE modes will degrade the grid's H-plane pattern by radiating from the edges of the array, and, on the other hand, TM modes will cause poor E-plane patterns.

Assuming each element is excited with equal phase, the power associated with the substrate modes can be expressed as [25]

$$P = K \int |EF|^2 |AF|^2 \, d\theta \tag{4.10}$$

where EF is the element factor, which is defined according to Fig. 4.18

$$EF = \sin\theta \quad \text{(TE modes)} \tag{4.11-a}$$

$$EF = \cos\theta \quad \text{(TM modes)} \tag{4.11-b}$$

and AF is the array factor, which is defined by

$$AF = \frac{\sin\left(\frac{M\beta U_x \cos\theta}{2}\right)}{\sin\left(\frac{M\beta U_x \cos\theta}{2}\right)} \frac{\sin\left(\frac{N\beta U_y \sin\theta}{2}\right)}{\sin\left(\frac{N\beta U_y \sin\theta}{2}\right)} \tag{4.12}$$

where U_x is the spacing between the elements in the x direction, U_y is the spacing between the elements in the y direction, and M and N are the number of elements in the x and y direction respectively, and K is the normalized power [26] for a single dipole antenna defined by

$$K_{TE} = \frac{3\lambda_0 \cos^2 \phi_{TE}}{4h_e} \tag{4.13-a}$$

$$K_{TM} = \frac{3\lambda_0 \sin^2 \phi_{TM} \cos^2 \theta_d}{4h_e} \tag{4.13-b}$$

for the TE and TM modes respectively, where ϕ_{TE}, ϕ_{TM}, and θ_d are given by Kogelnik [27].

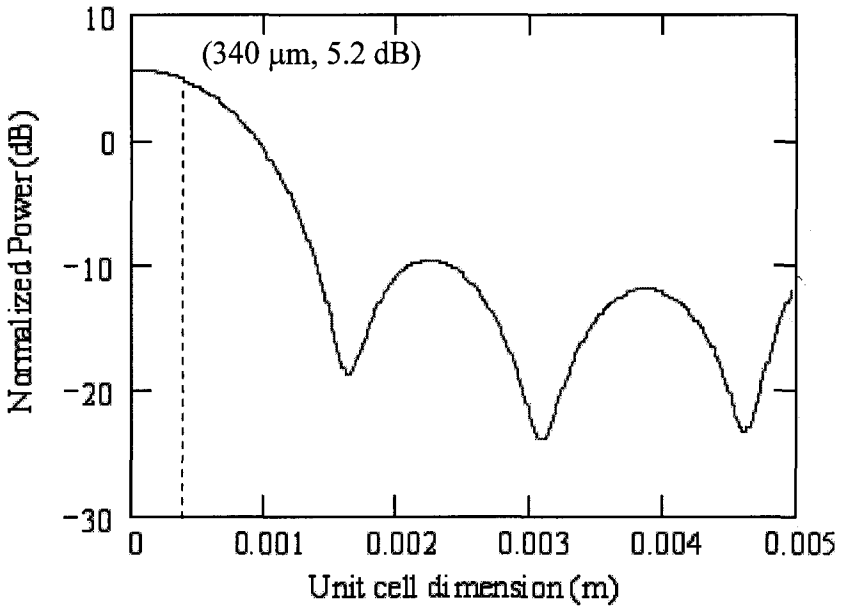
Substitute equations (4.11), (4.12) and (4.13) into equation (4.10), the substrate TE and TM mode power is given by

$$P_{TE} = K_{TE} \int_{-\pi}^{\pi} \sin^2\theta \bullet \left| \frac{\sin\left(\frac{M\beta U_x \cos\theta}{2}\right)}{\sin\left(\frac{\beta U_x \cos\theta}{2}\right)} \right|^2 \left| \frac{\sin\left(\frac{N\beta U_y \sin\theta}{2}\right)}{\sin\left(\frac{\beta U_y \sin\theta}{2}\right)} \right|^2 d\theta \tag{4.14-a}$$

$$P_{TM} = K_{TM} \int_{-\pi}^{\pi} \cos^2\theta \bullet \left| \frac{\sin\left(\frac{M\beta U_x \cos\theta}{2}\right)}{\sin\left(\frac{\beta U_x \cos\theta}{2}\right)} \right|^2 \left| \frac{\sin\left(\frac{N\beta U_y \sin\theta}{2}\right)}{\sin\left(\frac{\beta U_y \sin\theta}{2}\right)} \right|^2 d\theta \qquad (4.14\text{-b})$$

Now, consider the MMIC AlSb/InAs HEMT grid oscillator on a GaAs substrate designed for 50 GHz. For a 4 × 4 array of grid oscillator 50 GHz built on a grounded GaAs substrate with dielectric constant ε_r = 12.9 and 0.1 mm thick, there only the TM_0 mode exists, according to section 4.4.1. Thus the total substrate power is the power carried by TM_0 mode. Figure 4.19 shows how the normalized substrate mode power varies with the unit-cell size of the grid. Here, the unit cell is set as a square ($U_x = U_y$). For a grid with 340 μm × 340 μm unit-cell size, the substrate mode power is 5.2 dB higher than the power radiated into free space. Similarly, for a 6 × 6 array of MMIC AlSb/InAs grid oscillator with the same unit-cell size, the substrate mode power is 10.8 dB higher than the power radiated into free space.

Figure 4.19 indicates that the designed Q-band MMIC AlSb/InAs HEMT grid oscillator will have a good H-plane radiation pattern, since there is no TE substrate mode leaking from the vertical edges, while the TM_0 substrate mode radiating from the horizontal edges of the array will have negative impact on the E-plane pattern. It also predicts the 4 × 4 array will have a better E-plane pattern than the 6 × 6 array grid. Both plots in Fig. 4.19 suggest decreasing substrate-mode power with larger unit cell size. However, larger unit-cell dimensions decrease the operational frequency.



(a)

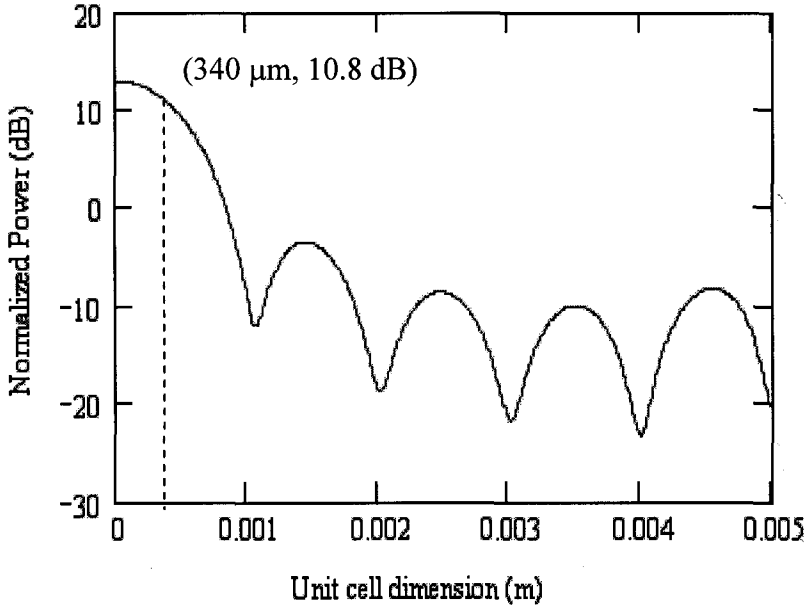


Fig. 4.19 Normalized total substrate-mode power vs. square unit cell dimension for (a) a 4 × 4 array; (b) a 6 × 6 array of grid oscillator at 50 GHz.

Besides the impact on radiation patterns, the substrate modes also affect the output power of the grid oscillator. For the 4.48-GHz C-band hybrid grid oscillator studied in the previous chapter, Fig. 4.20 shows the relationship between the normalized substrate mode power and the unit-cell size of the grid. At the designed 6-mm unit-cell size, the substrate mode power is 20.5 dB higher than the power radiated into free space. This can explain why the EIRP of this grid oscillator is not high. Similarly, the results in Fig. 4.20 predict the EIRP of the 50-GHz MMIC might be low.

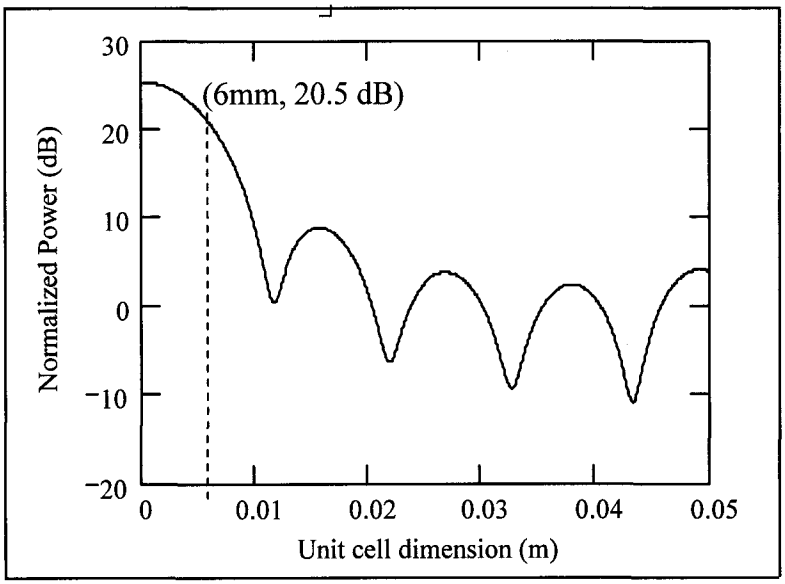


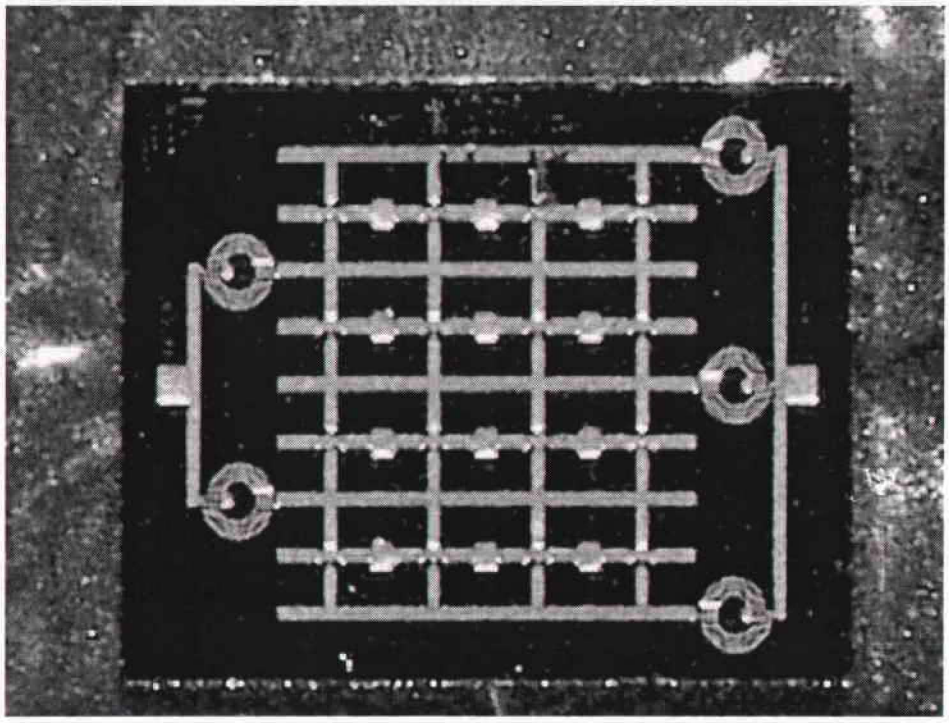
Fig. 4.20 Normalized total substrate-mode power vs. square unit cell dimension for the 4.48-GHz C-band hybrid grid oscillator in Chapter 3 with 6-mm unit-cell size.

4.5 Experimental Results

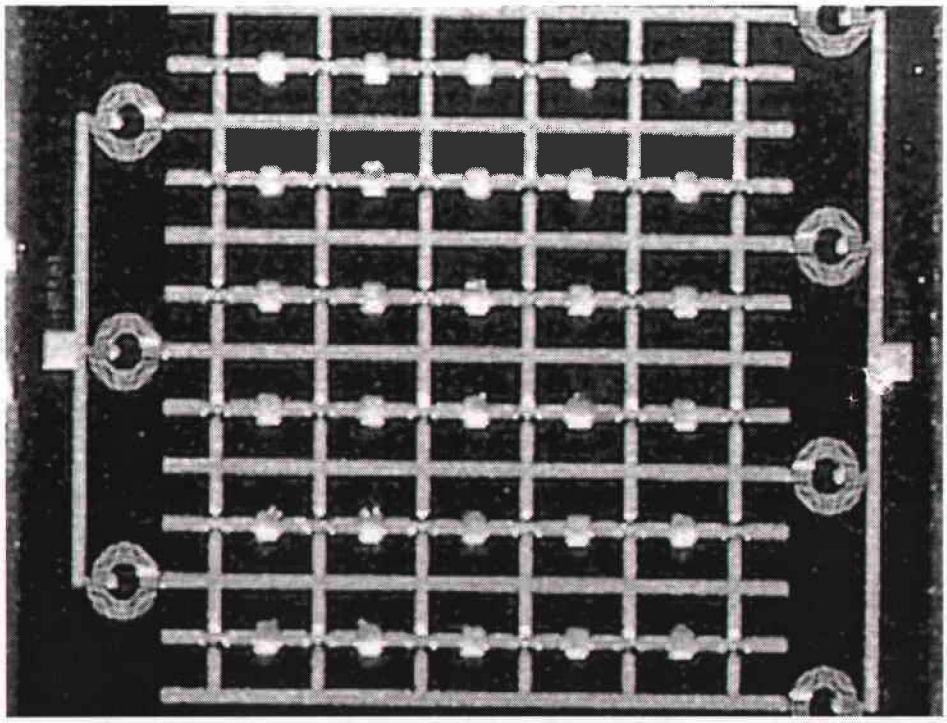
Two MMIC AlSb/InAs HEMT monolithic grid oscillators designed at 50 GHz were fabricated and tested. One of the grids consists of 16 (4×4 array), and the other one consists of 36 (6×6 array) AlSb/InAs HEMTs at intervals of 340 μm. The grid was built on a 100-μm-thick GaAs substrate with gold evaporated on the back side.

4.5.1 Monolithic Grid Fabrication

The fabrication of the monolithic grid was accomplished with the 0.15 μm baseline AlSb/InAs process compatible with the standard GaAs MMIC processes at NGST. The four-finger AlSb/InAs HEMTs have a gate length of 0.15 μm and a total gate width of 100 μm. According to NGST, the devices have a peak transconductance of 582.5 mS/mm and a corresponding current of 77.8 mA/mm at a gate bias of -0.38 V and a drain bias of 0.2 V. In addition to the HEMT fabrication, the grids require one extra mask step to lay out the connecting metal strips. To avoid the parasitics resulting from the cross-over of different metal layers, backside vias are used to ground the source of each device. To suppress RF signal in the horizontal metal strips, an inductor is placed at the end of each drain bias line and gate bias line individually. All of the drain bias lines are connected to a common bias pad, and so are the gate bias lines. The die size for the 4×4 grid is 1.8 mm × 2.1 mm, and for the 6×6 grid is 2.5 mm × 3.0 mm. The GaAs substrate is 100 μm thick, and the back surface is covered with gold to serve as the mirror and DC ground. Figure 4.21 (a) and (b) are the photographs of the 4×4 grid and the 6×6 grid, respectively.



(a)



(b)

4.21 Photograph of the Q-band AlSb/InAs HEMT monolithic grid oscillator: (a) 4x4 arrays, (b) 6x6 arrays. The unit cell size is 340 μm and all the metal strips are 34 μm.

4.5.2 Grid Assembly for Testing

For the convenience of the measurement, the grids were packaged at MMCOMM, Inc. The grids are mounted on a piece of gold-plated alumina with an area of 2.54 cm × 2.54 cm by silver epoxy EPO-TEK H20E cured at 140 °C for 10 min. To DC bias the grids, bond wires connect the bias pad to a chip capacitor first, and then a gold-plated substrate, both of which are mounted on the alumina by silver epoxy like the grids, and a wire is soldered on the stand, for both the drain side and gate side. Another wire is soldered on the alumina for the DC ground. The grid-mounted alumina is attached on a metal antenna range mounting fixture which was designed and fabricated for a standard radiation pattern measurement set-up at ANCOM, Inc. Figure 4.22 shows the assembled 4×4 grid.

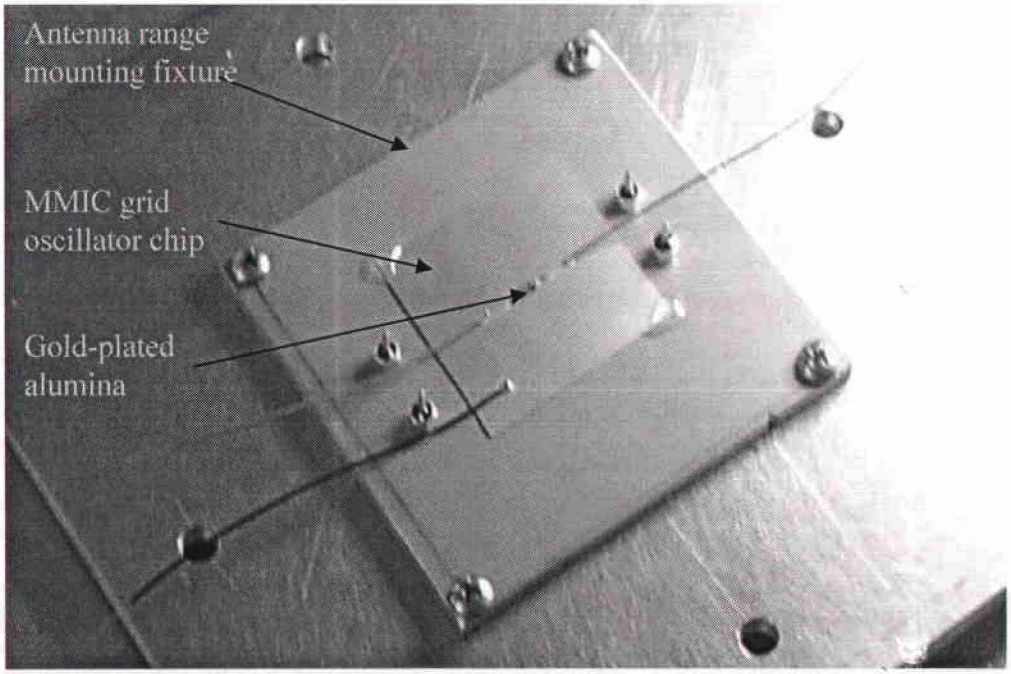
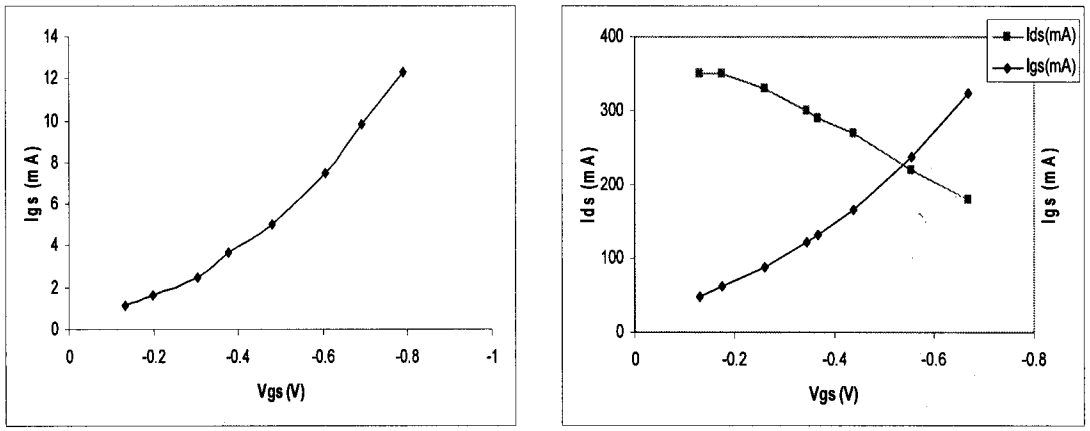


Fig. 4.22 Photograph of the grid mounted on a gold plated alumina which is attached on an antenna mounting fixture.

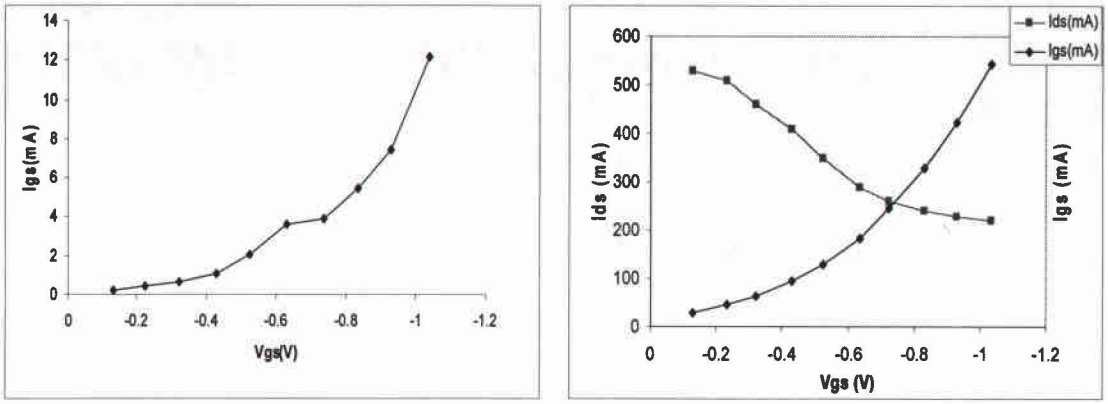
4.5.3 Experimental Results and Discussion for the First-Run Fabricated Grids

Figure 4.23 and 4.24 show the DC testing results for the 4×4 and 6×6 grid, respectively. For both grids, the gate current increases with the negative gate voltage when V_{ds} = 0 V, and no pinch-off was observed. According to NGST, pinch-off voltage for the device on the same wafer is supposed to be -0.675 V. According to the design, to observe 50-GHz oscillation, the devices on the grid should be biased at V_{gs} = -0.44 V and V_{ds} = 0.5 V with corresponding I_{ds} = 48 mA and 108 mA for 4×4 and 6×6 grid, respectively. On the contrast, I_{ds} = 270 mA for 4×4 grid and I_{ds} = 410 mA for 6×6 grid, much higher currents than expected were observed. At the same time, large gate leakage currents were found at this bias for both grids. These observations indicate there are failed devices in the grids. As a result, the RF performance cannot be evaluated since no oscillation was observed in the range of less than 75 GHz by using spectrum analyzer.



(a) (b)

Fig. 4.23 DC testing results for a 4×4-array grid: (a) Igs vs. Vgs at Vds = 0 V, (b) Ids and Igs vs. Vgs at Vds = 0.509 V.



(a) (b)

Fig. 4.24 DC testing results for a 6×6-array grid: (a) Igs vs. Vgs at Vds = 0 V, (b) Ids and Igs vs. Vgs at Vds = 0.498 V.

To find out why the grids did not perform as expected, the grids were brought under Olympus Vanox microscope. By examining the circuits carefully, several fabrication problems were observed, as shown in Fig. 4.25: (a) shorted drain and source; (b) lifted metal strips; (c) poor fabricated via.

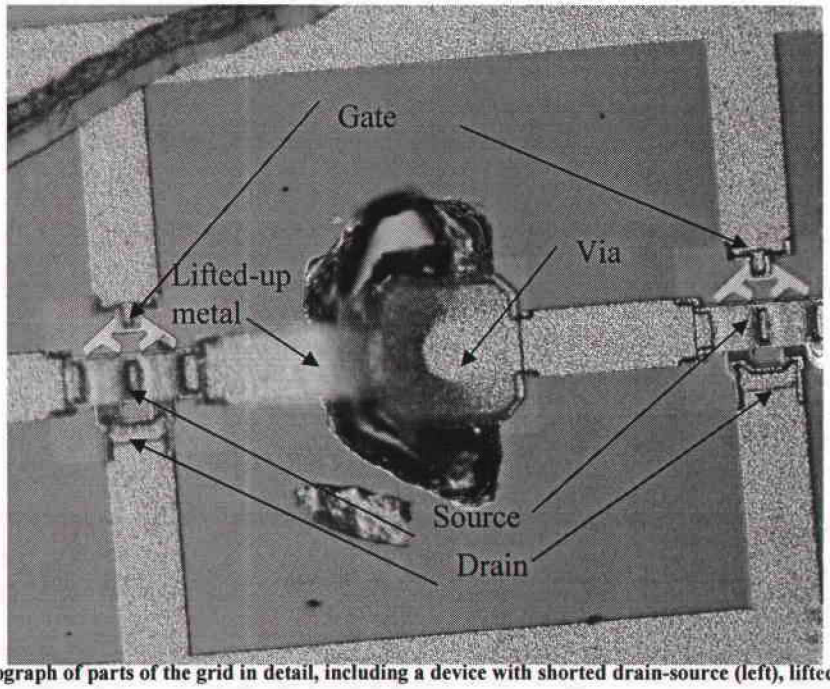


Fig. 4.25 Photograph of parts of the grid in detail, including a device with shorted drain-source (left), lifted-up metal and a poor-fabricated via. Picture was taken by using Olympus DP11.

The DC testing results and the observation under the microscope indicate the fabrication failure of some devices on the grid oscillator chips. Due to the non-yield of the devices, the RF performance of the two grid oscillators could not be evaluated.

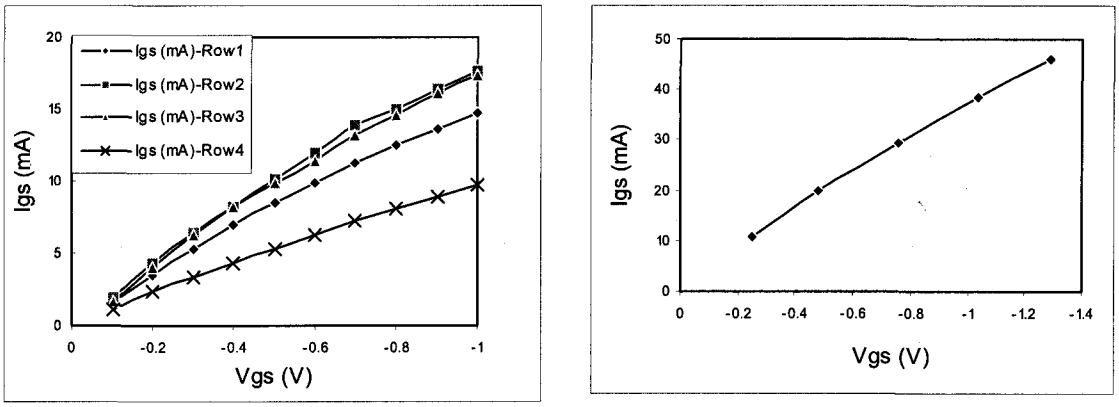
4.5.4 Experimental Results and Discussion for the Second-Run Fabricated Grids

The experimental results for the first-run fabrication indicated unresolved fabrication problems at the foundry. For the second-run fabrication, a modification to the layout was made to aid in troubleshooting. In the first run, one bias pad was provided for all gate lines and one bias pad for all drain lines. In the second run, a separate bias pad was provided for each bias line. This helps to identify failed devices in each row, and allows each row of transistors to be biased separately so that the failed devices don't impact the good devices in the other rows.

Even though some grid-chips fabricated in the second-run were found to have the same problems, such as the lift-up of metal strips and pads and poorly fabricated via, some looked good under the microscope. Those passing a visual test were assembled in the same way described in Section 4.5.2.

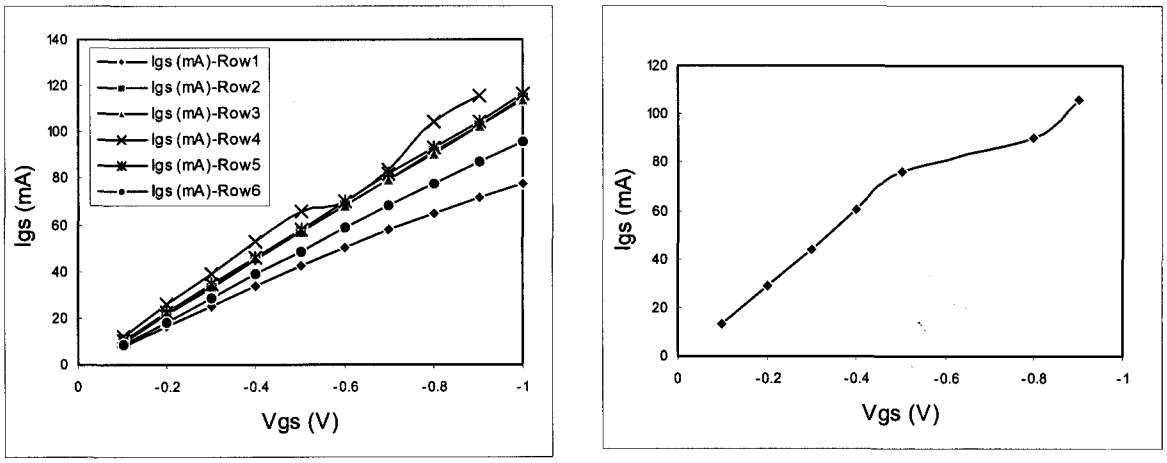
Figures 4.26 and 4.27 show the DC testing results for the 4×4 and 6×6 grid, respectively. As indicated in both figures, unfortunately the same problem of large gate-leakage currents was found during testing. For both grids, the gate current of each row and the whole array devices increases with the negative gate voltage when V_{ds} = 0 V, and no pinch-off was observed. Comparing Figure 4.26 (b) and 4.27 (b) with Figure 4.23 (a) and 4.24 (a) respectively, it is found that leakage current is even

much higher for the second-run fabricated chips than those in the first-run. These observations indicate though these chips looked good, there are failed devices in each row of the grids. As a result, the RF performance cannot be evaluated since no oscillation was observed in the range of less than 75 GHz using a spectrum analyzer.



(a) (b)

Fig. 4.26 DC testing results for a 4×4-array grid: Igs vs. Vgs at Vds = 0 V for (a) each row, (b) the whole 4×4 array.



(a) (b)

Fig. 4.27 DC testing results for a 6×6-array grid: Igs vs. Vgs at Vds = 0 V for (a) each row, (b) the whole 6×6 array.

4.6 Summary

This chapter presented the design, fabrication and experimental results of a MMIC AlSb/InAs HEMT grid oscillator with predicted 50-GHz operational frequency. The optimum circular function of this grid oscillator based on the optimum equivalent feedback circuit for the maximum oscillator power indicates it operates at the under-compression point. A substrate-mode analysis was also investigated. Due to the non-yield of the devices, the RF performance of the grid oscillator cannot be evaluated.

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Chapter 5 Conclusions and Future Work

5.1 Conclusions

The primary objective of this thesis is to design, fabricate and test the first MMIC AlSb/InAs HEMT grid oscillator. To meet this goal, the following work was presented in this thesis:

- Verified the validity of HFSS by comparing the simulated S-parameters with GAP results (Chapter 2).
- Designed and tested a C-band hybrid grid oscillator with holes through the substrate by using HFSS and ADS (Chapter 3).
- Designed a MMIC AlSb/InAs HEMT grid oscillator at 50 GHz (Chapter 4).
- Analyzed the operational point for the designed MMIC grid oscillator by using the theory of grid oscillator optimization (Chapter 4).
- Analyzed the impact of substrate modes on the radiation pattern for the designed MMIC grid oscillator (Chapter 4).
- Tested the MMIC grid oscillators and analyzed the failure reason (Chapter 4).

Based on this work, the following conclusions can be drawn:

- HFSS simulation result is trustworthy, but it is different from GAP which is more accurate.
- The C-band hybrid grid oscillator oscillated at 4.48 GHz, which is close to the predicted 4.6 GHz. Besides this oscillation frequency, oscillations at 5.35 GHz and 5.72 GHz were observed at varied dimensions due to edge effects. The

edge effect also had an impact on the EIRP and DC-to-RF conversion efficiency.

- By choosing model sdHCA4CKT-ms1_0 AlSb/InAs HEMTs and a unit-cell grid with dipole-dipole configuration and 340-μm unit-cell size, the design goal of 50-GHz operational frequency could be achieved.
- The optimum circular function associated with the equivalent circuit for the maximum output power for this design indicated it works at under-compression point, which implies the efficiency of grid oscillator are not high, and future works has to be done to increase the efficiency.
- The TM_0 substrate-mode power with this unit cell dimension was 5.2 dB and 10.8 dB higher than the power radiated into the free space for a 4×4 and a 6×6 arrays, respectively. It implies poor E-plane radiation pattern.
- The experimental result for both 4×4 and 6×6 MMIC AlSb/InAs HEMT grid oscillators showed they did not illustrate the expected DC characteristics due to the unresolved fabrication issues at the foundry. Therefore, their RF performance could not be evaluated.

5.2 Future Work

The problems met during the grid testing indicate that unresolved issues, such as poor metal adhesion to the substrate and large leakage gate-current, existed in the fabrication of the two prototype grid oscillators. To get high-quality grid oscillator chips, the foundry has to figure out how to fix these problems.

Besides the fabrication process, the optimum circular function suggests to redesign the grid unit cell to provide a proper feedback so that the designed grid oscillator works close to the optimum point. Since the fabrication process fixes the substrate thickness (100 μm), the unit-cell geometry has to be altered. The equivalent circuit synthesized for the maximum output power of the grid oscillator indicated an asymmetric unit cell can be used instead of symmetric dipole-dipole configuration. For example, a slot-dipole configuration [1] can be employed in the new design.

The substrate-mode power analysis also suggests new design has to be done to reduce the substrate-mode power. An electrical band gap structure (EBG) would be a promising candidate. The technique reduces the substrate mode power by utilizing the stop bands that occurs when the EBG period is one half-wavelength at the operating frequency. It has been found that using photonic band gap (PBG) structure as mirror for the grid oscillator [2] can produce higher radiated power. Similarly, EBG can be used as substrates to suppress the substrate-mode power.

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Appendix A

Simulated S-Parameters by using TRW's equivalent circuit model.

Device: HCA4CKT

$j := \sqrt{-1}$ $\quad Vds := 0.5\ V$ $\quad Zo := 50\ ohms$

$Ids := 3\ mA$ $\quad f := 50\ GHz$

$s11 := .771 \cdot \exp\left(-145.161 \cdot \frac{\pi}{180} \cdot j\right)$ $\quad s12 := .172 \cdot \exp\left(9.13 \cdot \frac{\pi}{180} \cdot j\right)$

$s21 := 1.428 \cdot \exp\left(76.987 \cdot \frac{\pi}{180} \cdot j\right)$ $\quad s22 := .464 \cdot \exp\left(170.512 \cdot \frac{\pi}{180} \cdot j\right)$

Compute the optimum gain compression for maximum oscillator power:

Small-signal maximum efficient gain:

$\Delta := |s11 \cdot s22 - s21 \cdot s12|$ $\quad \Delta = 0.320129$

$K := \frac{1 + \Delta^2 - (|s11|)^2 - (|s22|)^2}{2 \cdot |s12| \cdot |s21|}$ $\quad K = 0.595942$

$Go := \frac{\left(\left|\frac{s21}{s12}\right|\right)^2 - 1}{2 \cdot \left(K \cdot \left|\frac{s21}{s12}\right| - 1\right)}$ $\quad 10 \cdot \log(Go) = 9.35\ dB$

$Go = 8.603557$

Optimum maximum efficient gain:

$Gme := \frac{Go - 1}{\ln(Go)}$ $\quad 10 \cdot \log(Gme) = 5.48\ dB$

$Gme = 3.532963$

Optimum gain compression:

$10 \cdot \log\left(\frac{Go}{Gme}\right) = 3.87\ dB$

Reduce |s21| to achieve this amount of gain compression:

$Xc := .641$

$s21 := Xc \cdot s21$

$\Delta := |s11 \cdot s22 - s21 \cdot s12|$ $\Delta = 0.312657$

$K := \dfrac{1 + \Delta^2 - (|s11|)^2 - (|s22|)^2}{2 \cdot |s12| \cdot |s21|}$ $K = 0.914689$

$Gme := \dfrac{\left(\left|\dfrac{s21}{s12}\right|\right)^2 - 1}{2 \cdot \left(K \cdot \left|\dfrac{s21}{s12}\right| - 1\right)}$ $10 \cdot \log(Gme) = 5.48$ dB

$Gme = 3.531925$

Convert device s-parameters to y-parameters:

$del := (1 + s11) \cdot (1 + s22) - s12 \cdot s21$ $Yo := \dfrac{1}{Zo}$

$y11 := Yo \cdot \dfrac{(1 - s11) \cdot (1 + s22) + s12 \cdot s21}{del}$ $y12 := Yo \cdot \dfrac{-2 \cdot s12}{del}$

$y21 := Yo \cdot \dfrac{-2 \cdot s21}{del}$ $y22 := Yo \cdot \dfrac{(1 + s11) \cdot (1 - s22) + s12 \cdot s21}{del}$

Determine optimum two-port gain of the device network

$g11 := Re(y11)$ $g21 := Re(y21)$ $b12 := Im(y12)$

$g12 := Re(y12)$ $g22 := Re(y22)$ $b21 := Im(y21)$

Vehovec's version:

$Aopt := -\dfrac{y21 + \overline{y12}}{2 \cdot g22}$

$Aopt = -0.842 + 0.679j$

$Ar := Re(Aopt)$ $Ai := Im(Aopt)$

Synthesize optimum pi-embedding network (load in shunt with drain-to-gate)

$F1 := -Re(y11 + Aopt \cdot y12)$ $F3 := -Re(y21 + Aopt \cdot y22)$

$F2 := -Im(y11 + Aopt \cdot y12)$ $F4 := -Im(y21 + Aopt \cdot y22)$

$B1 := (F1 + F3) \cdot \dfrac{Ar}{Ai} + F2 + F4$

$$C1 := \frac{B1}{2\cdot\pi\cdot f\cdot 10^{9}\cdot 10^{-12}} \qquad C1 = 0.134 \text{ pF} \qquad L1 := \frac{-1}{2\cdot\pi\cdot f\cdot 10^{9}\cdot 10^{-9}\cdot B1} \qquad L1 = -0.08 \text{ nH}$$

$$B2 := \frac{-(F1 + F3)}{Ai}$$

$$C2 := \frac{B2}{2\cdot\pi\cdot f\cdot 10^{9}\cdot 10^{-12}} \qquad C2 = 0.2 \text{ pF} \qquad L2 := \frac{-1}{2\cdot\pi\cdot f\cdot 10^{9}\cdot 10^{-9}\cdot B2} \qquad L2 = -0.05 \text{ nH}$$

$$G3 := \frac{F1 + Ar\cdot F3 + Ai\cdot F4}{(|1 - Aopt|)^2} \qquad B3 := \frac{(Ar - 1)\left[F4 + \frac{Ar}{Ai}(F1 + F3)\right] + Ai\cdot F1}{(|1 - Aopt|)^2}$$

$$Z3 := \frac{1}{G3 + j\cdot B3}$$

$$R3 := Re(Z3) \qquad R3 = 3.94 \text{ ohms}$$

$$X3 := Im(Z3) \qquad L3 := \frac{X3}{2\cdot\pi\cdot f} \qquad L3 = 0.06 \text{ nH}$$

$$C3 := \frac{-1}{2\cdot\pi\cdot f\cdot 10^{9}\cdot X3\cdot 10^{-12}} \qquad C3 = -0.16 \text{ pF}$$

Calculate embedding network y-parameters:

$$Y1 := j\cdot B1 \qquad Y1 = 0.042131j$$

$$Y2 := j\cdot B2 \qquad Y2 = 0.063652j$$

$$Y3 := G3 + j\cdot B3 \qquad Y3 = 9.943105\times 10^{-3} - 0.049246j$$

$$w11 := Y1 + Y3 \qquad w12 := -Y3$$

$$w21 := -Y3 \qquad w22 := Y2 + Y3$$

Convert to embedding network s-parameters:

$$del := (w11 + Yo)\cdot(w22 + Yo) - w12\cdot w21$$

$$t11 := \frac{(Yo - w11)\cdot(Yo + w22) + w12\cdot w21}{del} \qquad t12 := \frac{-2\cdot w12\cdot Yo}{del}$$

$$t21 := \frac{-2\cdot w21\cdot Yo}{del} \qquad t22 := \frac{(Yo + w11)\cdot(Yo - w22) + w12\cdot w21}{del}$$

$|t11| = 0.627121$ $|t12| = 0.568567$

$\arg(t11)\cdot\frac{180}{\pi} = 176.474201$ $\arg(t12)\cdot\frac{180}{\pi} = -98.391606$

$|t21| = 0.568567$ $|t22| = 0.733647$

$\arg(t21)\cdot\frac{180}{\pi} = -98.391606$ $\arg(t22)\cdot\frac{180}{\pi} = -164.943602$

Calculate Mason denominator D, which is zero for an optimum embedding network.

$Ds := s11\cdot s22 - s12\cdot s21$

$Dt := t11\cdot t22 - t12\cdot t21$

$D := 1 - (s11\cdot t11 + s12\cdot t21 + s21\cdot t12 + s22\cdot t22) + Ds\cdot Dt$

$D = 0$

Calculate the optimum largel-signal circular function, Copt

$$Copt := \frac{s11\cdot t11 + s21\cdot t12 - Ds\cdot Dt}{1 - s12\cdot t21 - s22\cdot t22}$$

$Copt = 1$

$|Copt| = 1$

$\arg(Copt)\cdot\frac{180}{\pi} = -4.512819\times 10^{-15}$

Calculate the optimum small-signal circular function, Copt

$$s21 := \frac{s21}{Xc}$$

$$Copt := \frac{s11\cdot t11 + s21\cdot t12 - Ds\cdot Dt}{1 - s12\cdot t21 - s22\cdot t22}$$

$Copt = 1.391626 - 0.199618j$

$|Copt| = 1.405869$

$\arg(Copt)\cdot\frac{180}{\pi} = -8.162939$

Appendix B

Inputs

Frequency $f := 50 \cdot 10^{9}$

Thickness (meter) $d := 100 \cdot 10^{-3} \cdot 10^{-3}$ $d = 1 \times 10^{-4}$

Dielectric constant $\varepsilon r := 12.9$

Number of elements $N := 6$ $M := 6$

Dispersion relations for TE and TM modes in grounded substrate

$hd := (0, 0.00001 .. 1)$

$c := 3 \cdot 10^{8}$

$ko := \frac{2 \cdot \pi \cdot f}{c}$ $\lambda o := \frac{c}{f}$ $\lambda d := \frac{\lambda o}{\sqrt{\varepsilon r}}$

$ko = 1.047 \times 10^{3}$ $\lambda o = 6 \times 10^{-3}$ $\lambda d = 1.671 \times 10^{-3}$

$kd := ko \cdot \sqrt{\varepsilon r}$ $V := ko \cdot d \cdot \sqrt{\varepsilon r - 1}$ $pdcircle(hd) := \sqrt{V^2 - hd^2}$

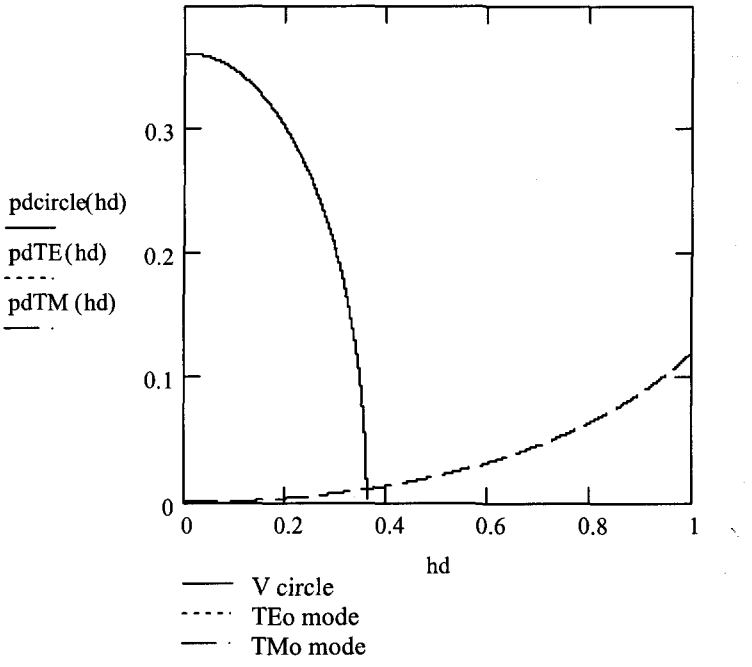
TE modes:

$pdTE(hd) := -hd \cdot \cot(hd)$

TM modes:

$pdTM(hd) := \frac{hd}{\varepsilon r} \cdot \tan(hd)$

Graphical representation of the dispersion relations for the modes that exist



There is only the TM0 mode exists.

For TE modes, calculate to find β

$TOL := 10^{-15}$ $\quad hdguess := 0.1$

$O(hd) := pdTE(hd) - pdcircle(hd)$

$hdTEo := root(O(hdguess), hdguess)$ Returns the value of hdguess to hdTEo, that makes O(hdguess)=0.

$hdTEo =$ ▮ Intersection point

$O(hdTEo) =$ ▮ Confirmed

$pdTE(hdTEo) =$ ▮ $\quad pdE := pdTE(hdTEo)$

$$\beta TE := \sqrt{\left(\frac{pdE}{d}\right)^2 + ko^2} \qquad \beta TE =$$ ▮

$hdTE := hdTEo$ $\quad \beta TE := \sqrt{kd^2 - \left(\frac{hdTE}{d}\right)^2}$ $\quad \beta TE =$ ▮

For TM modes, calculate to find β

$TOL := 10^{-15}$ $\quad hdguess := 0.38$

$k(hd) := pdTM(hd) - pdcircle(hd)$

$hdTMo := root(k(hdguess), hdguess)$

$hdTMo = 0.361$ Intersection point

$k(hdTMo) = 0$ To confirm

$pdTM := pdTM(hdTMo)$ $\quad pdTM = 0.011$

$$\beta TM := \sqrt{\left(\frac{pdTM}{d}\right)^2 + ko^2} \qquad \beta TM = 1.053 \times 10^3$$

$hdTM := hdTMo$ $\quad hdTM = 0.361$

$$\beta TM := \sqrt{kd^2 - \left(\frac{hdTM}{d}\right)^2} \qquad \beta TM = 1.053 \times 10^3$$

Substrate mode power for different unit cell size:

$Uy := 0.00001, 0.00002 .. 0.005$ Unit cell size sweep (assume a squre unit cell)

TE Modes

$\beta TE =$ ▮

$$heffTE := d + \frac{2}{\sqrt{\beta TE^2 - ko^2}} \qquad heffTE = ▮$$

$$hTE := \sqrt{\beta TE^2 - ko^2} \qquad kcTE := \sqrt{\varepsilon r^2 \cdot ko^2 - \beta TE^2}$$

$$\phi TE := atan\left(\frac{hTE}{kcTE}\right)$$

$$KTE := \frac{3 \cdot \lambda o \cdot \cos(\phi TE)^2}{4 \cdot heffTE} \qquad TOL := 10^{-4}$$

Substrate mode power for TEo mode:

$$PTE(Uy) := 10\cdot\log\left[KTE\cdot\int_{-\pi}^{\pi}\left(\frac{\left|\sin\left(\frac{M\cdot\beta TE\cdot Uy\cdot\cos(\theta)}{2}\right)\right|}{\left|\sin\left(\frac{\beta TE\cdot Uy\cdot\cos(\theta)}{2}\right)\right|}\right)^2\cdot\left(\frac{\left|\sin\left(\frac{N\cdot\beta TE\cdot Uy\cdot\sin(\theta)}{2}\right)\right|}{\left|\sin\left(\frac{\beta TE\cdot Uy\cdot\sin(\theta)}{2}\right)\right|}\right)^2\cdot(\sin(\theta))^2\,d\theta\right]$$

TM modes

$$\beta TM = 1.053\times 10^3$$

$$heffTM := d + \frac{1}{\sqrt{\beta TM^2 - ko^2}}\cdot\left[\frac{1}{\left(\frac{\beta TM}{kd}\right)^2 + \left(\frac{\beta TM}{ko}\right)^2 - 1}\right] \qquad heffTM = 0.107$$

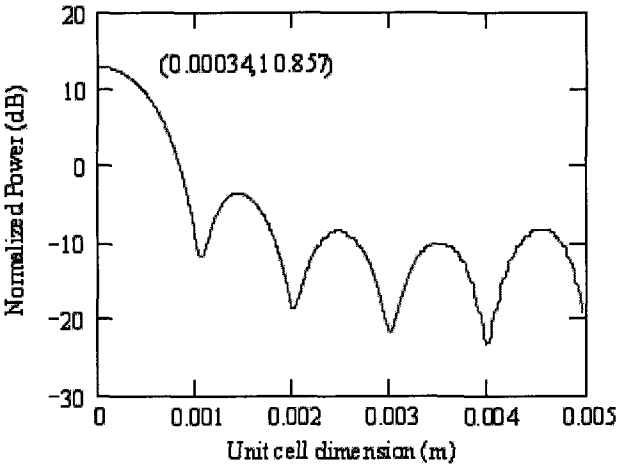
$$hTM := \sqrt{\beta TM^2 - ko^2} \qquad kcTM := \sqrt{\varepsilon r\cdot ko^2 - \beta TM^2}$$

$$\theta d := asin\left(\frac{\beta TM}{ko\cdot\sqrt{\varepsilon r}}\right) \qquad \phi TM := atan\left(\frac{\varepsilon r\cdot hTM}{kcTM}\right)$$

$$KTM := \frac{3\cdot\lambda o\cdot\sin(\phi TM)^2\cdot\cos(\theta d)^2}{4\cdot heffTM}$$

Substrate mode power for TMo mode:

$$PTM(Uy) := 10\cdot\log\left[KTM\cdot\int_{-\pi}^{\pi}\left(\frac{\left|\sin\left(\frac{M\cdot\beta TM\cdot Uy\cdot\cos(\theta)}{2}\right)\right|}{\left|\sin\left(\frac{\beta TM\cdot Uy\cdot\cos(\theta)}{2}\right)\right|}\right)^2\cdot\left(\frac{\left|\sin\left(\frac{N\cdot\beta TM\cdot Uy\cdot\sin(\theta)}{2}\right)\right|}{\left|\sin\left(\frac{\beta TM\cdot Uy\cdot\sin(\theta)}{2}\right)\right|}\right)^2\cdot(\cos(\theta))^2\,d\theta\right]$$



Substrate mode power for TMo as a function of elements spacing