DESIGN OF FRONT-END AMPLIFIER FOR OPTICAL RECEIVER IN 0.5 MICROMETER CMOS TECHNOLOGY

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Abstract

The need for high speed optical receivers are being driven by high speed and wide bandwidth optical communications demands. The front-end amplifier is a critical part in optical receiver. Traditionally, it has been fabricated in expensive Gallium Arsenide and silicon bipolar technologies. However, the quest for low cost, low power consumption and small silicon area solutions in the commercial market has spurred a desire to implement the circuit in Complementary Metal Oxide Semiconductor (CMOS) technology.

This thesis describes the design of the front-end amplifier using AMI 0.5 CMOS process. The target data rate is at least 500Mb/s suitable for local area network application. The front-end amplifier is divided into two stages, the transimpedance amplifier (TIA) and the limiter amplifier (LA). The resistive feedback TIA topology is selected for the TIA design. The LA circuit is realized by cascading two resistive load differential amplifiers with one buffer.

The simulation results show that the designed TIA achieves 374.4MHz bandwidth with a corresponding achievable data rate of ~ 535Mb/s. Its transimpedance gain is 4 kΩ . The LA bandwidth is 586.8MHz and the output swing is 4.2V.

The fabricated TIA and the front-end amplifier are experimentally tested to validate performance in the frequency range up to 24MHz. The simulation and the experimental results exhibit good agreement at these frequencies.

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Chapter 1. Introduction

Fiber optical communication system plays an important role in present communication industry. It offers several advantages including low cost, small size, low transmission loss and high bandwidth compared to conventional electrical communication based on Copper. It is widely used in high-speed, wide-bandwidth applications such as local area networks (LANs) and fiber to home (FTTH) [1, 2]. Its architecture is illustrated in Figure 1.1.

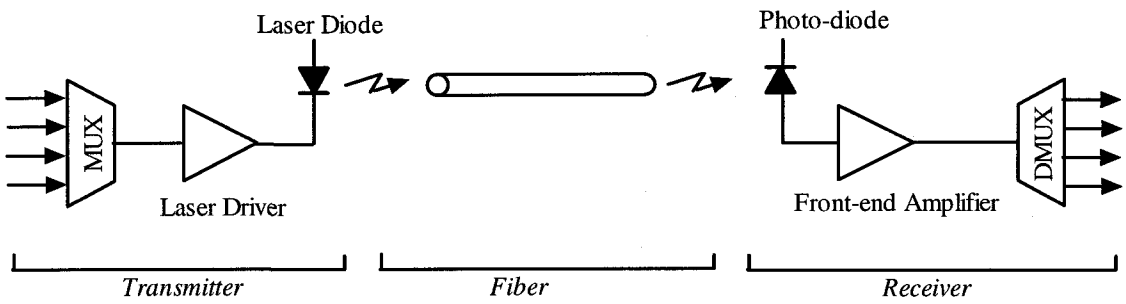

Figure 1.1 Fiber optical system

It consists of a transmitter, a fiber and a receiver. The modulation of the electrical signal to light takes place at the level of the transmitter. Relatively low-speed parallel electrical signals are transformed to high-speed serial signal by a multiplexer (MUX). Subsequently, the electrical signal is fed to the laser driver and light is produced by the laser diode according to the input current. After this transmitter stage, the light is carried

to a remote destination by the fiber. The conversion of the incoming light back to electrical signals takes place at the side of the receiver. There, a photodiode converts the incoming light to current. Next, a front-end amplifier converts the current back to an electrical signal. Finally, a demultiplexer (DMUX) transfers the series data back to parallel data [3].

The project addressed in this thesis is the design of a front-end amplifier. The amplifier consists of two stages, as shown in Figure 1.2. The first stage is a transimpedance amplifier (TIA), and the second stage is a limiting amplifier (LA).

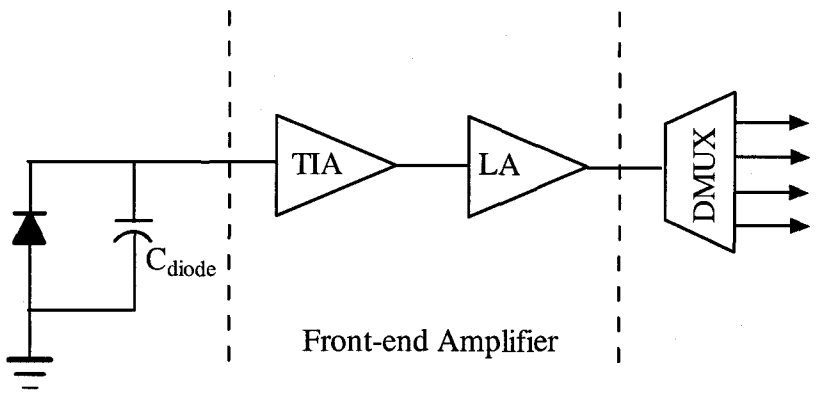

Figure 1.2 Front-end amplifier composed of TIA and LA stages

The TIA is the most critical part of an optical receiver design because its noise, gain and frequency performance largely determines the overall data rate that can be achieved in an optical system. The function of a TIA is to convert the input current from the

external photodiode to a voltage output. The TIA has a large transimpedance gain and a low sensitivity to the photodiode capacitance. These characteristics are important because the input photocurrent is very small, typically varying from about 10μA to 20μA . In addition, the photodiode capacitance is usually large, ranging from about 0.3pF to 1pF [4,5,6,7].

Although the structure of TIA offers large gain, the signal produced by TIA still suffers from small amplitude, usually on the order of a few tens of millivolts. Therefore, the TIA must be followed by a LA, which boosts the voltage swing and matches the output impedance to drive the DMUX [2].

There are several competing technologies such as Silicon Bipolar (Si-bipolar), Gallium Arsenide (GaAs), Silicon Germanium (SiGe), Silicon-On-Insulator (SOI) and Complementary Metal Oxide Semiconductor (CMOS) to design front-end amplifiers. Table 1.1 lists several front-end amplifiers which are reported in the literature [1,7,8,9,10,11]. The technologies of Si-bipolar, GaAs, SiGe and SOI offer large bandwidth transistors. Therefore it is easier to design high speed front-end amplifier using these processes than to design it using CMOS technology. However, the needs for low cost, low power consumption and small silicon area have motivated front-end amplifier to be implemented in CMOS. CMOS technology offers System-On-Chip (SOC) solution because it can integrate the analog and digital components on a same chip. In addition, the performance of CMOS technologies is being improved constantly and consistently. In fact, submicrometer CMOS technologies now exhibit sufficient performance for radio-frequency applications in the 1-2GHz range and higher.

Process	Feature Size	Data Rate
Si-bipolar	0.3 μm	5Gb/s
GaAs	0.5 μm	1.7Gb/s
SiGe	0.5 μm	2Gb/s
SOI	0.5 μm	700Mb/s
CMOS	0.6 μm	250Mb/s
CMOS	0.35 μm	2.5Gb/s

Table 1.1 Front-end Amplifier Fabricated in Different Technology

The objective of this thesis project is to design a front-end amplifier in CMOS technology. The data rate is aimed to be larger than 500Mb/s so that it is comparable with current LAN data rates and sufficiently fast to support real-time video applications. The circuits are fabricated in AMI 0.5 μm C5N (AMI05), which is a 5-Volt, N-Well process. It has three metal layers, two poly layers, and a high resistance layer. Stacked contacts are supported. In this process, the minimum allowable drawn length is 0.6 μm while its effective gate length is 0.5 μm.

This thesis consists of five chapters. Chapter 2 illustrates and compares several possible topologies for TIA. It also examines the design issues of LA. Chapter 3 describes the implementation of TIA and LA circuits using AMI 0.5 μm CMOS technology. Additionally, it shows the layout of the front-end amplifier system. Chapter

4 illustrates the simulation results and experiment tests. Chapter 5 is the conclusion of the thesis with suggestions for future design considerations.

Chapter 2. Literature Review

Many papers in literature present the different topologies of the TIA and LA circuit design using CMOS process. This chapter summarizes several design topologies which are widely used. The concerns and motivations involved in the TIA and the LA circuit design are also presented.

2.1 TIA Performance Parameters

As previously mentioned, the TIA is the most critical part of an optical receiver. The main design challenges are trade-offs between transimpedance gain, bandwidth and input noise current. Before examining the TIA design topologies, a brief description of these parameters is presented below.

2.1.1 Bandwidth

The bandwidth of a TIA determines the data rate of an optical receiver. For a non-return to zero (NRZ) data format, the bandwidth should be set to 0.7 times the data rate [1,12]. This result is due to the compromise between the intersymbol interference (ISI) and noise. In order to achieve better performance for NRZ data, the bandwidth should be maximized to reduce the ISI. On the contrary, the bandwidth cannot be too large because while a TIA amplifies the signal, it also amplifies the noise at different frequency as well. According to this rule, because the desired data rate of this thesis project is 500Mb/s, the bandwidth of the TIA should set to be larger than 350MHz.

$$f_{-3dB} = \text{Datarate} \times 0.7 = 500 \times 0.7 = 350\text{MHz} \qquad (2.1)$$

2.1.2 Transimpedance Gain

The transimpedance gain is the ratio of the output voltage amplitude over the input current amplitude at low frequency. It is given by

$$R_T = \frac{V_{out}}{I_{in}} \tag{2.2}$$

The gain of the TIA is expected to be as large as possible to enhance the sensitivity of the system. However, the gain is limited by the supply voltage headroom. Additionally, the gain cannot be too large in order to achieve large bandwidth. For example, the gain of the TIA may only be 530 Ω in order to achieve high bandwidth of 1.75GHz with supply voltage of 3V [1].

2.1.3 Input-referred Noise

The parameter of the input-referred noise is used to compare the noise generated by different TIA circuits. It is a fictitious quantity which cannot be observed in a circuit. This parameter does not depend on the gain of the TIA. As defined in [3], "input-referred noise is the value that, if applied to the input of the equivalent noiseless circuit, produces an output noise equal to that of the original, noisy circuit."

To illustrate how to calculate the input-referred noise, a TIA and its equivalent circuit is shown in Figure 2.1. The transimpedance gain is equal to R_L. We assume that the thermal noise of R_L is the only source of noise. The noise per unit bandwidth is given by

$$\overline{I_n^2} = \frac{4kT}{R_L} \tag{2.3}$$

where k is the Boltzmann's constant and T is the temperature of the circuit.

The output integrated noise is given by

$$\overline{V_{n,out}^2}=\int_0^{\infty}\frac{4kT}{R_L}\left|R_L\|\frac{1}{C_D j2\pi f}\right|^2 df=\frac{kT}{C_D} \tag{2.4}$$

Because the TIA has a transimipedance gain of R_L, its total input-referred noise current is equal to

$$\overline{I_{n,in}^2}=\frac{\overline{V_{n,out}^2}}{R_L^2}=\frac{kT}{R_L^2 C_D} \tag{2.5}$$

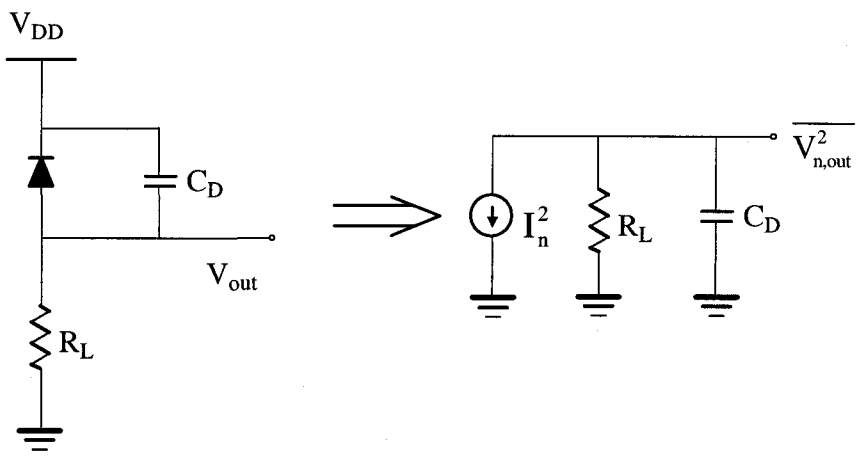

Figure 2.1 A TIA circuit and its equivalent circuit

The input-referred noise generated from the TIA directly determines the signal to noise ratio (SNR) of the optical network as indicated in the following equation

$$SNR=\frac{I_{in}}{I_{n,in}} \tag{2.6}$$

where I_{in} is the input current and $I_{n,in}$ is the input-referred noise. Because large SNR is desired in optical network, the TIA circuit which offers small input-referred noise is usually preferred.

2.2 TIA Design Topologies

There are many topologies of the TIA developed in order to achieve large transimpedance gain, large bandwidth and small input-referred noise. Three topologies are widely used, including the common-gate TIA, the resistive feedback TIA and the capacitive feedback TIA. These topologies are presented and their input-referred noises are compared. The inductive peaking topology is discussed later as an effective method of bandwidth enhancement.

2.2.1 Common-gate TIA

The common-gate (CG) amplifier stage is widely used in the open loop TIA topology since it exhibits low input impedance. The circuit is illustrated in Figure 2.2. The M1 transistor offers the common-gate gain. The M2 transistor supplies bias current for the M1 transistor. In order to simplify the AC signal analysis, only the diode capacitance is taken into account because it is quite larger than other parasitic capacitance values. In addition, the body effect of the transistor M1 is neglected. Under these assumptions, the transfer function is given by

$$\frac{V_{out}}{I_{in}} = \frac{g_{m1}R_D}{g_{m1}+C_D s} \tag{2.7}$$

Substituting s=0 in Eq (2.7), we find that the DC transimpedance gain can be written as

$$R_T = R_D \tag{2.8}$$

The bandwidth is given by

$$f_{-3dB} = \frac{g_{m1}}{2\pi C_D} \tag{2.9}$$

where the g_{m1} is the transconductance of the M1 transistor.

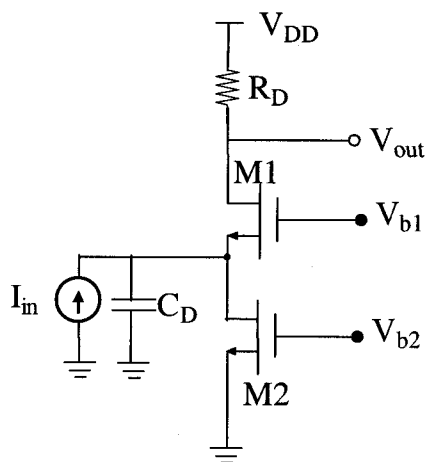

Figure 2.2 Common-gate TIA

The common-gate TIA is able to provide a large transimpedance gain and broad bandwidth. However, its input-referred noise is relatively large because the noise currents due to the transistor M_2 and the resistor R_D are directly referred to the input. It is given by

$$\overline{I_{n,in}^2} = I_{n,R_D}^2 + \overline{I_{n,M_2}^2} = \frac{4kT}{R_D} + 4kT\gamma g_{m2} \tag{2.10}$$

where γ is the threshold voltage parameter of the M2 transistor.

The design of the common-gate TIA has several constraints. According to Eq (2.9), in order to increase the bandwidth, the quantity of g_{m1} must be maximized. In other words, the width or the bias current of the M1 transistor should be increased. In the first situation, if the width is increased, the parasitic capacitance of the M1 transistor will also increase such that it will eventually limit the bandwidth. In the second situation, if the bias current is increased, the voltage drop across R_D must increase, requiring a greater supply voltage. In addition, if M2 transistor is made wider, it brings more noise to the TIA because it makes the second term of Eq (2.10) larger [5].

2.2.2 Resistive Feedback TIA

The topology of the resistive feedback TIA is demonstrated in Figure 2.3. It uses a resistor to sense the voltage at the output and returns a proportional current to the input. The transfer function is given by

$$\frac{V_{out}}{I_{in}} = -\frac{R_F}{1+\frac{R_F C_D}{A}s} \tag{2.11}$$

The transimpedance gain is given by

$$R_T = R_F \tag{2.12}$$

The bandwidth is given by

$$f_{-3dB} \approx \frac{A}{2\pi R_F C_D} \tag{2.13}$$

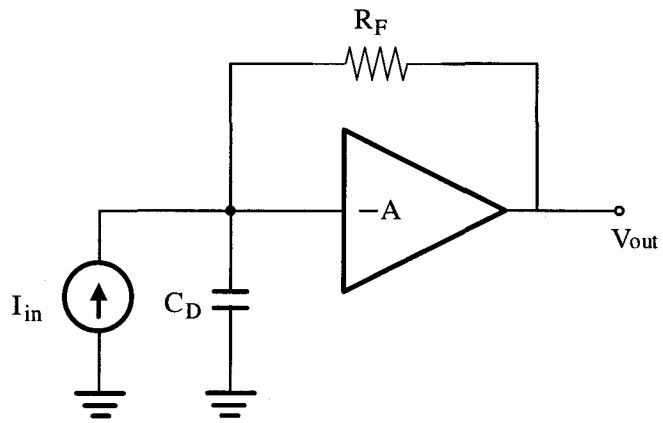

Figure 2.3 Resistive feedback TIA

The input noise current is given by

$$\overline{I_{n,in}^2} = \frac{4kT}{R_F} + \frac{\overline{V_{n,A}^2}}{R_F^2} \tag{2.14}$$

The first term is the noise of R_F which is directly referred to the input. The second term is the noise from the amplifier stage.

Eq (2.10) and Eq (2.14) reveal the critical difference between the input-referred noise between the CG TIA and the resistive feedback TIA. Although the first term in both equations plays the same role indicating the resistor thermal noise, the second term is not the same. In the resistive feedback TIA, if the R_F is large enough, the second term in Eq (2.14) may be quite smaller than the second term in Eq (2.10). It is a practical approach because the R_F resistor does not carry any bias current and its value does not limit the supply voltage headroom. Therefore, the resistive feedback TIA is able to offer smaller noise than the CG TIA.

The implementation of the resistive feedback TIA is illustrated in Figure 2.4. The M1 transistor acts as the amplifier stage, and M2 supplies bias current for the M1 transistor. The open-loop gain is given by

$$A=g_{m1}R_D \tag{2.15}$$

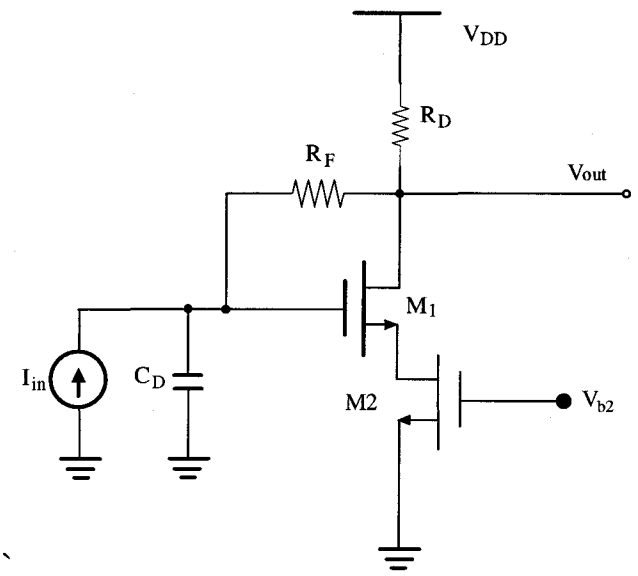

Figure 2.4 Implementation of resistive feedback TIA

The circuit suffers from one drawback. The bandwidth is limited because the value of R_D is limited by supply voltage. The voltage drop across R_D cannot exceed V_{DD}-V_{GS2}-V_{GS1}. Therefore, the R_D resistance has to be relatively small. The open-loop gain cannot be very large. According to Eq (2.13), the bandwidth is also limited [13, 14].

2.2.3 Capacitive Feedback TIA

Figure 2.5 illustrates the capactive feedback TIA, where C_1 senses the voltage across C_2 and returns a proportional current to the input. If the open-loop gain of the amplifier stage satisfies A>>1, then the ratio of the output current to the input current is given by

$$\frac{I_{out}}{I_{in}}=1+\frac{C_2}{C_1} \tag{2.16}$$

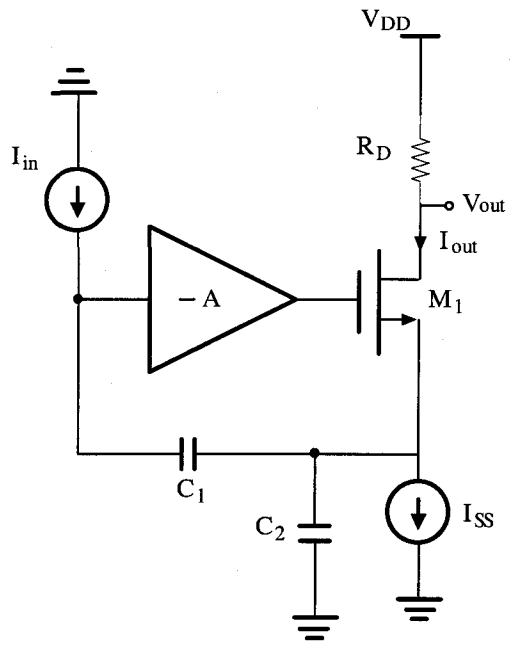

Figure 2.5 TIA with Capacitive feedback

It suggests that the circuit can operate as a current amplifier. With a resistor R_D tied to the drain of the M_1 transistor, it provides a transimpedance of

$$R_T=(1+\frac{C_2}{C_1})R_D \tag{2.17}$$

The bandwidth of the circuit is given by

$$f_{-3dB}=\frac{(1+A)g_{m1}}{2\pi C_2} \tag{2.18}$$

The input-referred noise is given by

$$\overline{I_{n,in}^2}=\frac{4kT}{R_D}+\frac{\overline{V_{n,A}^2}(C_2s)^2}{(1+\frac{C_2}{C_1})^2} \tag{2.19}$$

The first term is the noise of R_D which is directly referred to the input. The second term is the noise from the amplifier stage.

For fair comparison of the input-referred noises generated by the capacitive feedback TIA and the resistive feedback TIA, it is assumed that both circuits have the same gain. In other words, we have

$$R_F=(1+\frac{C_2}{C_1})R_D \tag{2.20}$$

By substituting the Eq (2.20) to Eq (2.14), the input-referred noise of the resistive feedback TIA is given by

$$\overline{I_{n,in}^2}=\frac{4kT}{R_D}+\frac{\overline{V_{n,A}^2}(\frac{1}{R_D})^2}{(1+\frac{C_2}{C_1})^2} \tag{2.21}$$

At low frequency, when $|C_2s|<\frac{1}{R_D}$, the capacitive feedback TIA generates smaller noise than the resistive feedback TIA. However, when the frequency increases so that $|C_2s|>\frac{1}{R_D}$, the resistive feedback TIA offers smaller noise [15]. Although this topology is

able to supply high transimpedance gain, it is able to achieve low noise only at low frequency.

In summary, among the three topologies as discussed above, the resistive feedback TIA offers the smallest noise at high frequency. Therefore, it is selected for the TIA circuit design in the thesis project.

2.2.4 Inductive Peaking

The limitation of the bandwidth of TIA is primarily due to the large capacitance either at the input or the output nodes. Therefore, if an inductor is inserted to resonate with the capacitance, the bandwidth can be enhanced. This method is called "inductive peaking", and may be applied to the three topologies discussed above. There are two types of inductive peaking, series peaking and shunt peaking.

Series Inductive Peaking

Series inductive peaking utilizes the inductor series with the input of the TIA. An example of the resistive feedback TIA with series inductive peaking is shown in Figure 2.6. The transfer function is given by [3]

$$\frac{V_{out}}{I_{in}} = -\frac{1}{s^2+\frac{R_F}{(A+1)L}s+\frac{1}{C_D L}} \bullet \frac{AR_F}{(A+1)C_D L} = -\frac{AR_F}{(A+1)C_D L} \bullet \frac{1}{s^2+2\zeta\omega_n s+\omega_n^2} \tag{2.22}$$

where $\zeta=\frac{R_F\sqrt{C_D L}}{2(A+1)L}$ and $\omega_n^2=\frac{1}{C_D L}$. If we set $\zeta=\sqrt{2}/2$ then the bandwidth of the TIA is given by

$$f_{-3dB} = \frac{\sqrt{2}A}{2\pi R_F C_D} \tag{2.23}$$

Hence, the bandwidth is increased by approximately 41% with an overshoot of 4.3%.

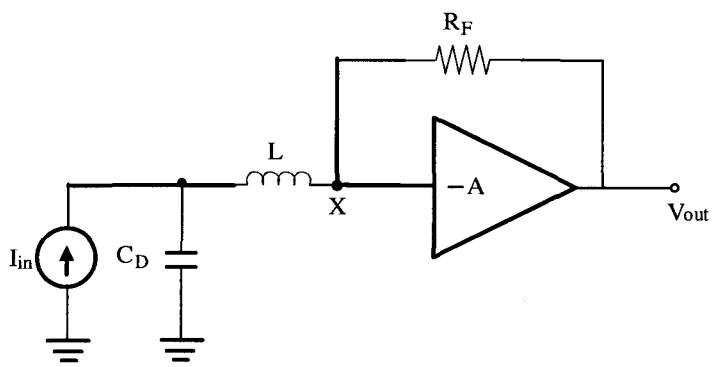

Figure 2.6 Resistive feedback TIA with series inductive peaking

However, series inductive peaking suffers from the requirement of using very large inductor, usually on the order of 1uH. The monolithic inductor cannot offer this large value. Therefore, it is possible to use a bond wire instead, which means that the length and shape of the wire and the capacitance of the photodiode must be controlled tightly.

Shunt Inductive Peaking

Shunt inductive peaking occurs when the inductor appears in parallel with the output. An example of common-source TIA with shunt inductive peaking is illustrated in Figure 2.7. In order to simplify the analysis, only the output capacitance is taken into account.

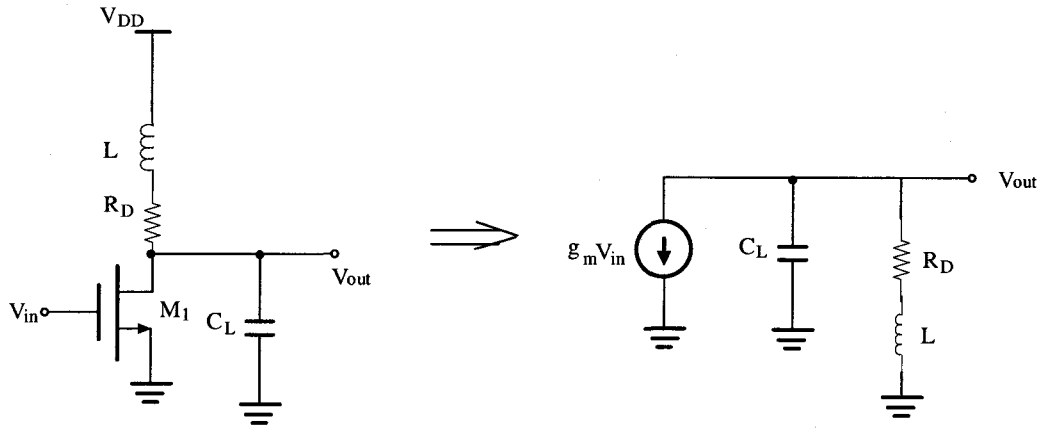

Figure 2.7 The common-source TIA with shunt inductive peaking

The transfer function is given by [3]

$$\frac{V_{out}}{V_{in}} = -g_m \frac{Ls+R_D}{LC_L s^2+R_D C_L s+1} = -g_m R_D \frac{s+2\zeta\omega_n}{s^2+2\zeta\omega_n s+\omega_n^2} \bullet \frac{\omega_n}{2\zeta} \tag{2.24}$$

where $\zeta=\frac{R_D}{2}\sqrt{\frac{C_L}{L}}$ and $\omega_n^2=\frac{1}{LC_L}$

The bandwidth is

$$f_{-3dB} = \frac{\zeta^2}{\pi R_D^2 C_L^2}[\frac{1}{4\zeta^2}+1-2\zeta^2+\sqrt{(\frac{1}{4\zeta^2}+1-2\zeta^2)+1}] \tag{2.25}$$

Table 2.1 demonstrates the bandwidth enhancement ratios and overshoot values according to different values of ζ. With the margin requirement for process and temperature variation, an overshoot of 7.5% offers a reasonable compromise between the control over the step response and the improvement in bandwidth. Therefore, according to Table 2.1, the bandwidth can be enhanced by 82% [16].

ζ	0.69	0.64	0.59
Bandwidth enhancement	78%	82%	84%
Overshoot	5%	7.5%	10%

Table 2.1 Characteristics of inductive peaking

2.2.5 Recently Reported TIA circuits

Table 2.2 summarizes several recent reported CMOS TIA circuits using the topologies discussed above.

	Technology	Supply	Topology	Bandwidth	Gain
Design in [5]	0.8 μm	5V	Common-Gate	950MHz	100Ω
Design in [4]	0.7 μm	5V	Resistive Feedback	1.5GHz	1kΩ
Design in [15]	0.6 μm	3V	Capacitive Feedback	550MHz	6.7kΩ
Design in [16]	0.6 μm	5V	Shunt Inductive Peaking	1.2GHz	1.6kΩ

Table 2.2 Recent reported CMOS TIA circuits

2.3 LA Performance Parameters

The bandwidth and the output swing are two critical parameters for the LA circuit design. Unlike the TIA, whose bandwidth should set to be approximately 70% of the data rate, the bandwidth of the LA is designed to be equal to the data rate. This is because if

two stages with equal bandwidths are cascaded, then the overall small-signal bandwidth is narrower.

The output swing of the LA must be large enough to drive the following DMUX stage. It must be at least 250mV. In some optical receiver circuits, it may be as large as full rail-to-rail swing [3, 4, 12].

2.4 LA Design Topologies

The cascaded gain stages are used to implement the role of a limiter amplifier. In order to understand the properties of LA, the performance of the cascaded gain stages is studied. Later, the circuit of the gain stage is demonstrated.

2.4.1 Cascaded Gain Stages

As illustrated in Figure 2.8, two gain stages are cascaded. Assuming they have the same voltage gain A_0, output resistance R_{out} and load capacitance C_L, the overall transfer function is given by [3]

$$H(s)=\left[\frac{A_0}{1+\frac{s}{\omega_0}}\right]^2 \tag{2.26}$$

where $\omega_0=\frac{1}{R_{out}C_L}$ is the -3dB bandwidth of each stage. Therefore, the bandwidth is given by

$$\omega_{-3dB}=\omega_0\sqrt{\sqrt{2}-1}\approx 0.644\omega_0 \tag{2.27}$$

From Eq (2.27), we know that cascading two identical stages decreases the bandwidth by about 36%. Similarly, for N identical stages, the -3dB bandwidth is given by

$$\omega_{-3dB}=\omega_0\sqrt{\sqrt[N]{2}-1} \tag{2.28}$$

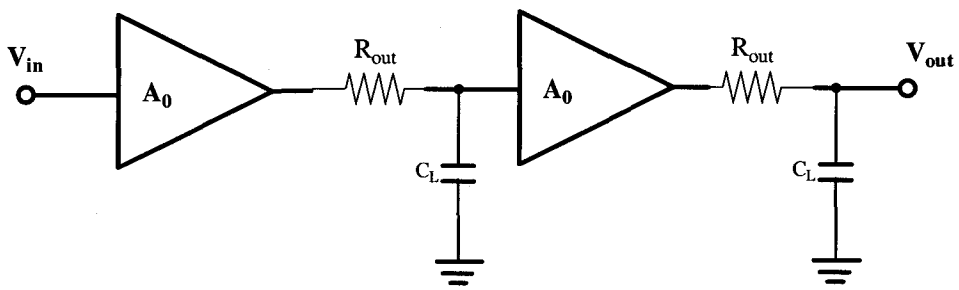

Figure 2.8 Cascade of small-signal amplifiers

Table 2.3 illustrates the ratio of the overall bandwidth over the single stage bandwidth as a function of N. Typically limiter amplifier employs no more than five gain stages due to the rapid decrease of overall bandwidth as increasing the number of gain stages.

N	2	3	4	5
$\frac{\omega_{-3dB}}{\omega_0}$	0.63	0.53	0.45	0.4

Table 2.3 The ratio of ω_{-3dB} over ω_0 as of N

In order to know the output swing of the LA, we need to examine the total gain of the LA. It is given by

$$A_{total}=(A_0)^N \tag{2.29}$$

This result from small-signal analysis only offers a conservative estimation for the output swing of the LA. Typically, the second or third gain stage of the LA senses sufficiently large input swing so that it operates in the switching state. Therefore, it is able to offer large output swing.

2.4.2 Resistive Load Differential Amplifier

The simplest circuit for the gain stage is resistive load different amplifier. The circuit is shown in Figure 2.9. Due to the symmetry of the design, the small signal performance can be analyzed with the aid of half-circuit model as illustrated in Figure 2.10.

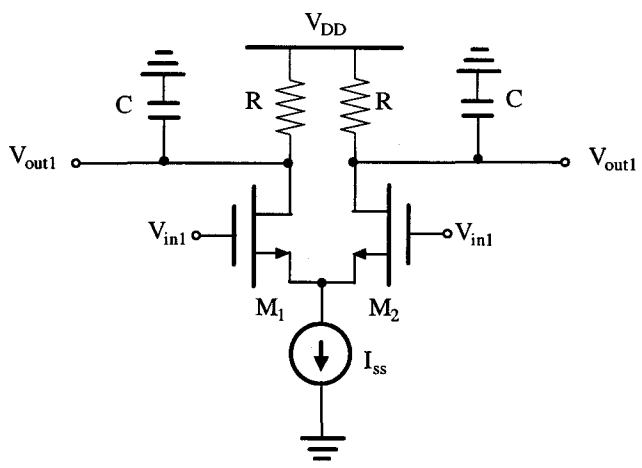

Figure 2.9 Resistive Load Differential Amplifier Schematic

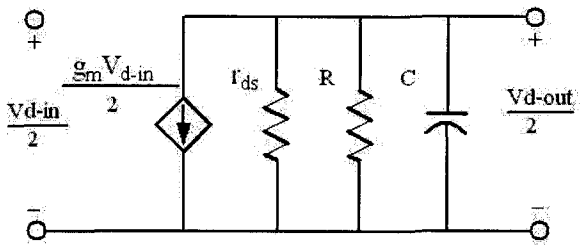

Figure 2.10 Small-signal model of differential half-circuit

The gain expression is [12]

$$A=g_m(r_{ds}//R) \approx g_m R \tag{2.36}$$

The bandwidth is

$$f_{-3dB}=\frac{1}{2\pi RC} \tag{2.37}$$

By cascading several resistive load differential amplifiers, a LA is shown as Figure 2.11. As can be seen, because the last stage is operated in non-linear region, the small signal can be converted into large output swing signal exhibiting short rise and fall time.

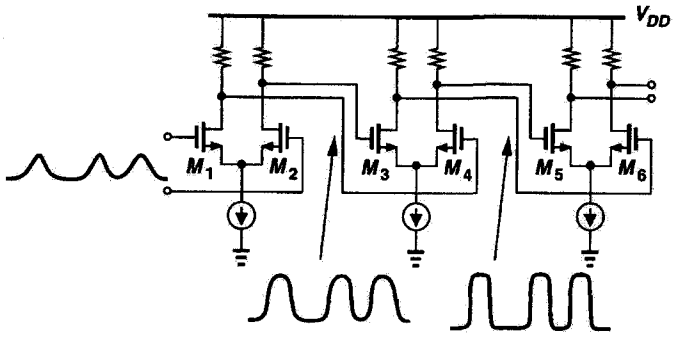

Figure 2.11 LA configuration

2.4.3 Recently Reported LA circuits

Several recent reported CMOS LA circuits using the topology discussed above are summarized in Table 2.4.

	Technology	Supply	Bandwidth	Output Swing
Design in [12]	0.18 μm	3.3V	1.1GHz	300mV
Design in [7]	0.5 μm	3.3V	1GHz	3.1V
Design in [17]	0.35 μm	5V	1.4GHz	280mV

Table 2.4 Recently reported CMOS LA circuits

Chapter 3. Thesis Project Circuit Design

This Chapter illustrates the implementation details of the front-end amplifier using the AMI05 process. First the design tools and the circuit design flow are introduced. Followed by that is the detailed design issues on the TIA and the LA circuits. Finally, the circuit layout is presented.

3.1 Design Tools and Design Flow

The circuit design is done using the Cadence Design Environment (CDE) and NCSU design kit. CDE is an Electronic Design Automation (EDA) environment, which integrates different tools for integrated circuit (IC) design together in a single framework. Therefore, it is able to support all the stages of an IC design.

NSCU Design Kit is supplied by North Carolina State University. It is a set of configuration and technology-related files to customize the design environment for the AMI05 process. The files includes layer definitions, parasitic capacitance, layout cells, simulation parameters, the rules for Design Rule Check (DRC) and the rules for Layout versus Schematic (LVS) verification.

The flow chart for the circuit design is shown in Figure 3.1. First, the specifications for the circuit such as the bandwidth are determined. Next, the parameters of the circuit such as the resistor value are set according to the results of hand calculation. Subsequently, a schematic view of the circuit is created using the Cadence Composer followed by the circuit simulation using Spectre. After the circuit specifications are satisfactorily met, the circuit layout is created using the Virtuoso Layout Editor.

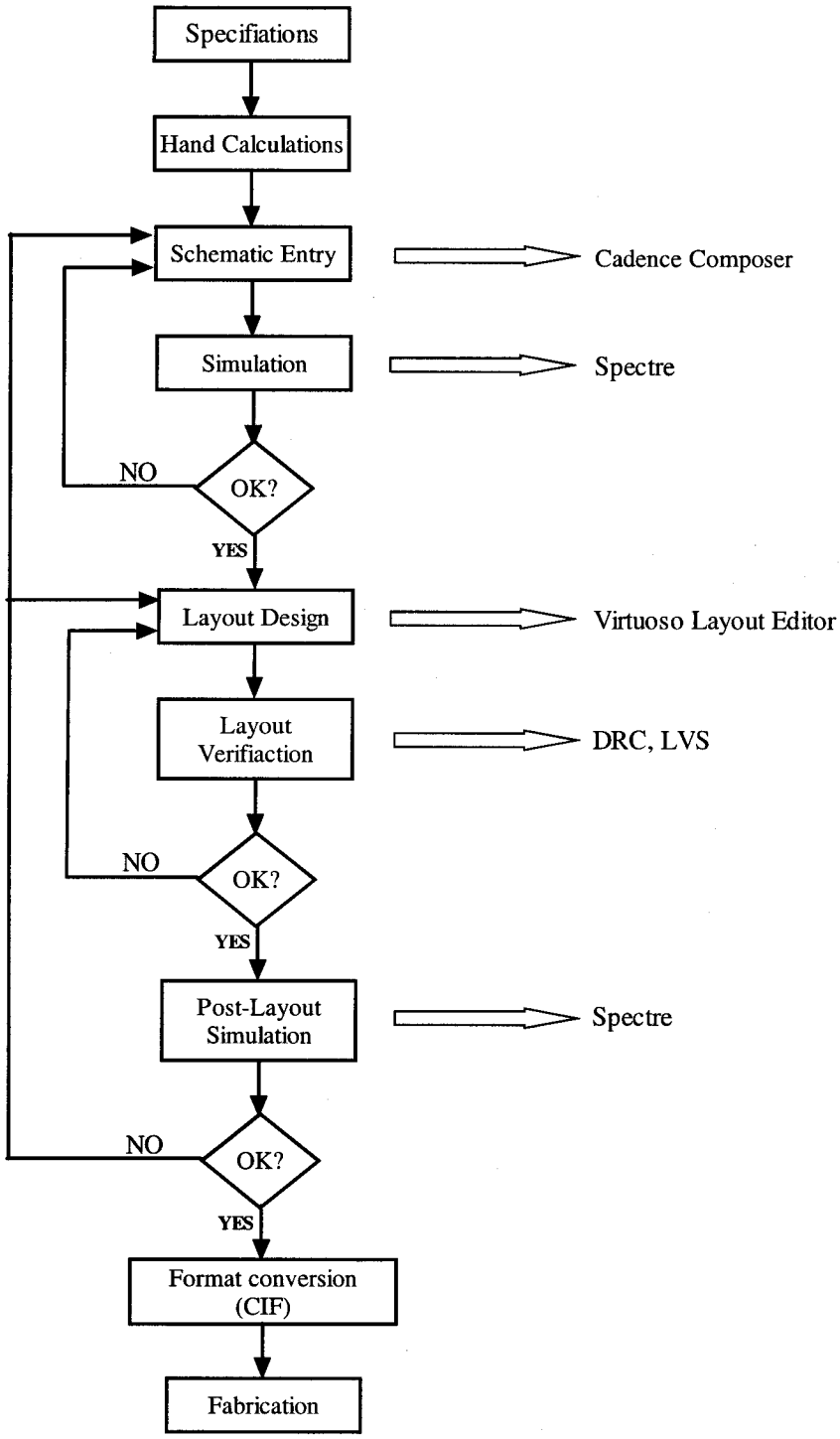

Figure 3.1 The Circuit Design Flow

The DRC verifies whether the layout satisfies the geometric constrains of the AMI05 process. The LVS compares the layout to the schematic to ensure that the intended functionality is implemented. If the layout passes the DRC and LVS check, post-simulation is carried by plugging the parasitic capacitors of the layout into the original schematic. After the results of the post-simulation meet the circuit specification, the layout is converted to CIF format and sent to be fabricated.

3.2 Definitions of Specifications

Figure 3.2 illustrates the block diagram of the front-end amplifier designed in the project. As previously mentioned, the data rate of the front-end amplifier should be larger than 500Mb/s. For TIA, the bandwidth should be larger than 350MHz. For LA, the bandwidth should be larger than 450MHz.

A photodiode is expected to produce a $20\,\mu A_{p\text{-}p}$ current signal. The TIA should amplify the current signal to be larger than $60\,mV_{p\text{-}p}$. Therefore, the transimpedance gain of TIA should be larger than $3\,k\Omega$. The LA should be able to boost the swing to 3.5V at least in order to drive the DMUX.

Throughout the following documentation, the circuit design will be verified with the specifications listed in Table 3.1.

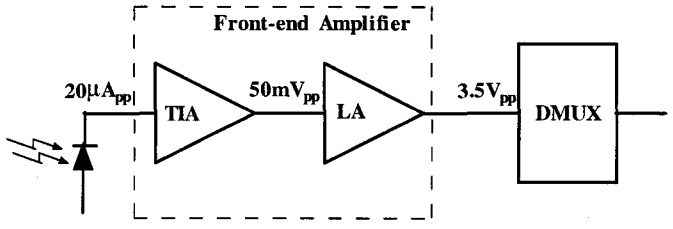

Figure 3.2 Front-end Amplifier Block Diagram

Parameter	*Value*
Minimum Data Rate	500Mb/s
TIA Minimum Bandwidth	350MHz
TIA Minimum Gain	3 kΩ
LA Minimum Bandwidth	450MHz
LA Minimun Output Swing	3.5V
Diode Light Current, i_D	20 μA
Diode Capacitance, C_D	0.5pF

Table 3.1 Proposed Front-end Amplifier Specifications

3.3 TIA Circuit Design

As mentioned in the previous chapter, the TIA circuit is designed using the resistive feedback topology. This topology is chosen because it generates the smallest noise while it offers high impedance gain and acceptable bandwidth. Additionally, it does not need to use any capacitor or inductor, which the AMI05 process can not supply.

Although the inductive peaking topology cannot be implemented due to the limitation of the AMI05 process, it is still studied in the simulation level because it is an effective way to enhance the bandwidth.

3.3.1 Schematic and Parameters

The TIA schematic is shown in Figure 3.3. The TIA circuit is based on the circuit as illustrated in Figure 2.4. However, it is modified to differential circuit in order to

suppress the fluctuations of power supply and substrate noise. The R1 resistor and M1, M2 transistors forms a current mirror to supply a constant current flow for the differential circuits. The transistors of M3, M4, M5 and M6 are differential pairs of resistive feedback TIA. The M3 and M5 transistors act as common-source amplifier to provide the voltage gain. The R_f resistors offer resistive feedback. The diode-connected PMOS transistors, M4 and M6, are used as load resistors. All the transistors have a gate length of $0.6\,\mu m$. The rest of the circuit parameters are listed as Table 3.2.

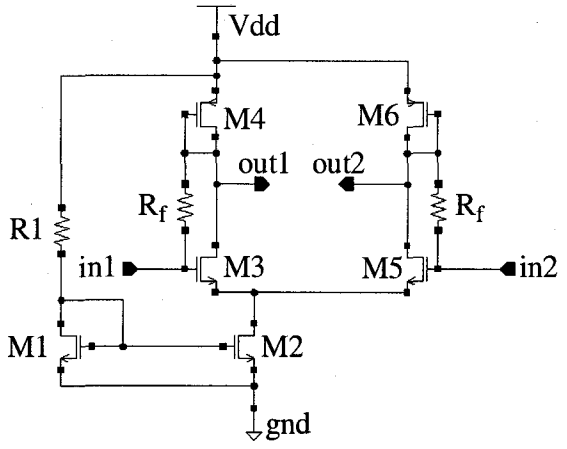

Figure 3.3 Resistive Feedback TIA schematic

M1	M2	M3	M4	M5	M6	R1	Rf
9μm	9μm	138μm	3μm	138μm	3μm	10.61kΩ	4.53kΩ

Table 3.2 TIA circuit parameters

3.3.2 Circuit Implementation

The AC half-circuit of the differential TIA is shown in Figure 3.4. M4 can be viewed as a resistor load. The value of the resistor is

$$R_D = \frac{1}{g_{m4}} \tag{3.1}$$

where the g_{m4} is the transconductance of M4 PMOS.

The voltage gain of the common source amplifier is given by

$$A = -\frac{g_{m3}}{g_{m4}} = -\sqrt{\frac{\mu_n (\frac{W}{L})_3}{\mu_p (\frac{W}{L})_4}} \tag{3.2}$$

where the μ_n and μ_p are the mobility of the electron and holes respectively.

As discussed in Chapter 2, the bandwidth of the resistive feedback TIA is

$$f_{-3dB} \approx \frac{1}{2\pi} \frac{A}{R_F C_D} \tag{3.3}$$

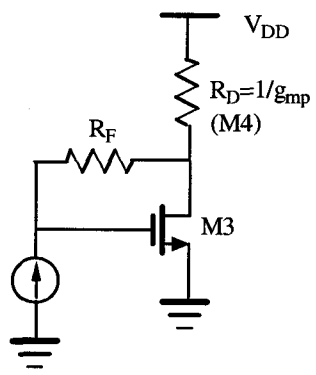

Figure 3.4 AC Half-circuit of TIA

According to Eq (3.3), the voltage gain should be set as large as possible to enhance the bandwidth. In other words, from Eq (3.2), the width of the M3 transistor should be set as large as possible if the width of the M4 is set to its minimum width. However, as the width of M3 increases, its gate-source capacitance, C_f, becomes so large that the Eq (3.3) is no longer valid. The bandwidth of TIA is given by

$$f_{-3dB} \approx \frac{1}{2\pi} \frac{A}{R_F(C_D + C_f)} \tag{3.4}$$

Therefore, the width of M3 cannot be too large due to the combined influences of the voltage gain and gate-source capacitance on bandwidth. Based on the result of simulation, the bandwidth of TIA reaches 374.4MHz when the width of M3 is set to be $138\,\mu m$.

As previously mentioned in Chapter 2, the transimpedance gain of the TIA is given by

$$\frac{V_{out}}{I_{in}} \approx -R_f \tag{3.5}$$

The simulation results show that when R_f is set to $4.5\,k\Omega$, the achieved transimpedance gain is $4\,k\Omega$. The output swing of the TIA is 80mV. In conclusion, the simulation results of bandwidth and gain meet the specifications for the TIA circuit.

3.3.3 Inductive Peaking

Series inductive peaking and shunt inductive peaking are both verified at the simulation level. While keeping the same circuit parameters as resistive feedback TIA, two inductors are added at the input nodes and at the output nodes respectively. The two circuits are illustrated in Figure 3.5 and Figure 3.6. Their simulation results and discussion are presented in the next chapter.

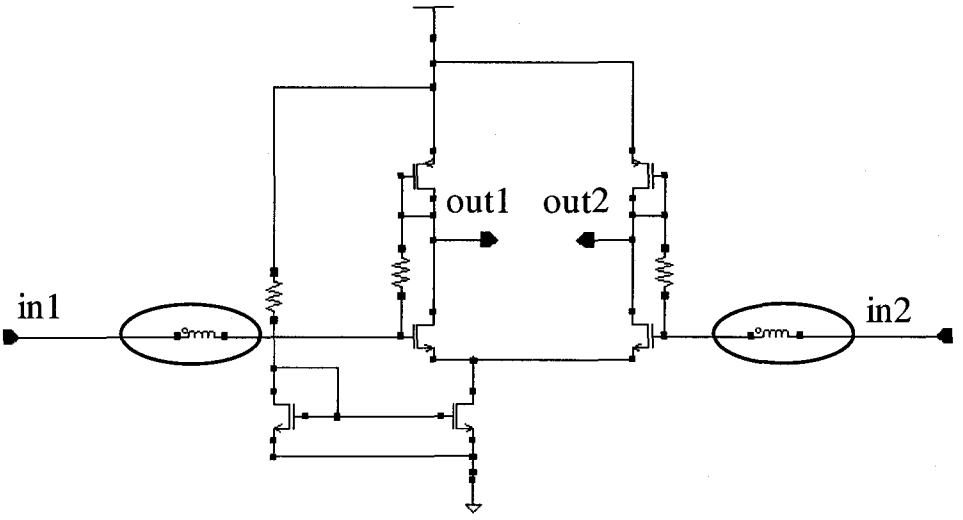

Figure 3.5 Series Inductive Peaking

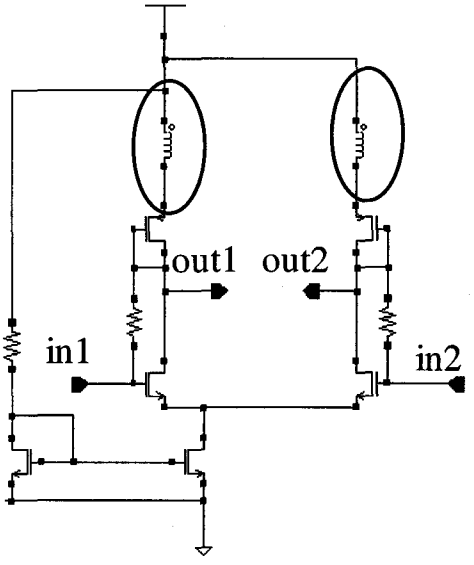

Figure 3.6 Shunt Inductive Peaking

3.4 LA Circuit Design

The LA circuit is implemented by cascading two stages of resistive load differential amplifiers and one stage of buffer as shown in Figure 3.7. The resistor R1 and transistors M1, M2, M7 and M12 form current mirrors to provide bias current for the differential amplifiers. All the transistors lengths are set to be $0.6\mu m$. The rest of the parameters of the LA circuit are listed in Table 3.3.

M1	M2	M7	M12	M3,M5,M8, M10,M13,M15	M4,M6,M9, M11,M14,M16	R1
9μm	12μm	24μm	36μm	6μm	3μm	10.61kΩ

Table 3.3 the parameters of LA circuit

The voltage gains of the two resistive load differential amplifiers are the same, given by

$$A=\frac{g_{m3}}{g_{m4}}=\sqrt{\frac{\mu_n(\frac{W}{L})_3}{\mu_p(\frac{W}{L})_4}}=2 \tag{3.6}$$

Therefore, two stages of differential amplifiers boost the output swing of the TIA from 80mV to 320mV. This output swing is large enough to drive the buffer working in saturation region. Therefore, the buffer offers large output swing. Moreover, the function of the buffer is to convert the differential outputs to single-ended output. The simulation result shows that the bandwidth of the LA is 586.8MHz and the swing is 4.2V, which satisfy our design specifications.

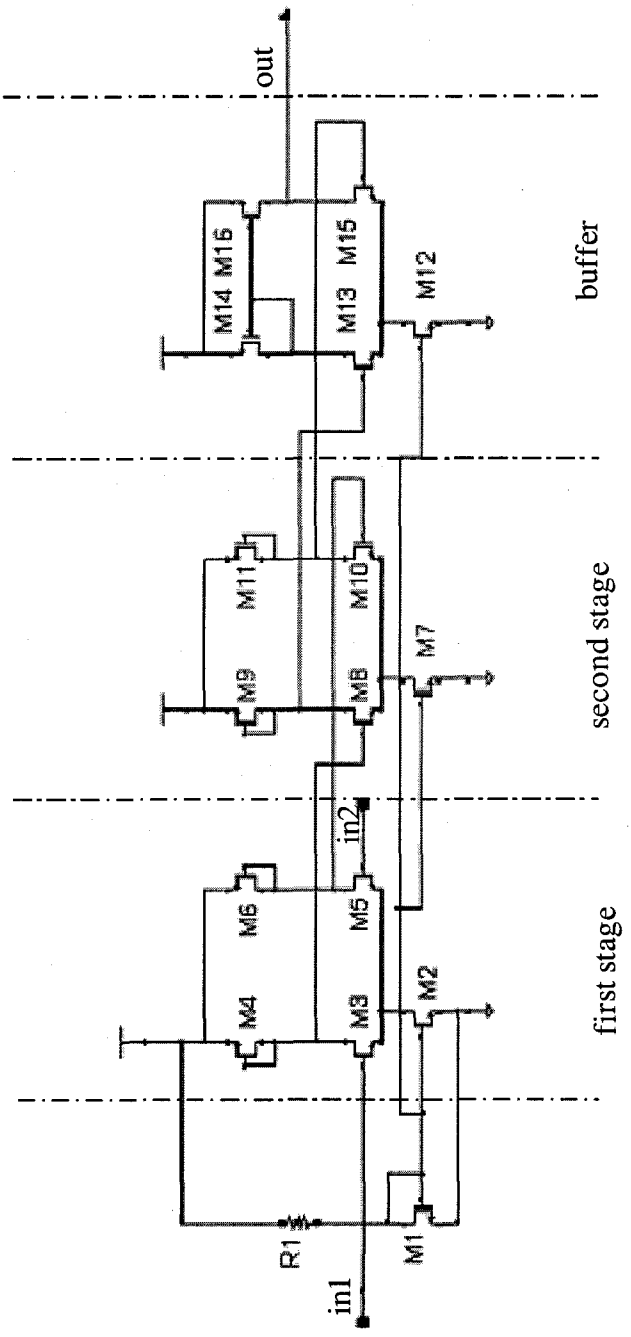

Figure 3.7 LA circuit

3.5 Front-end Amplifier Circuit

Since The TIA and LA circuit already meet the design specification, these two stage can be cascaded together to form the front-end amplifier. The circuit is shown in Figure 3.8.

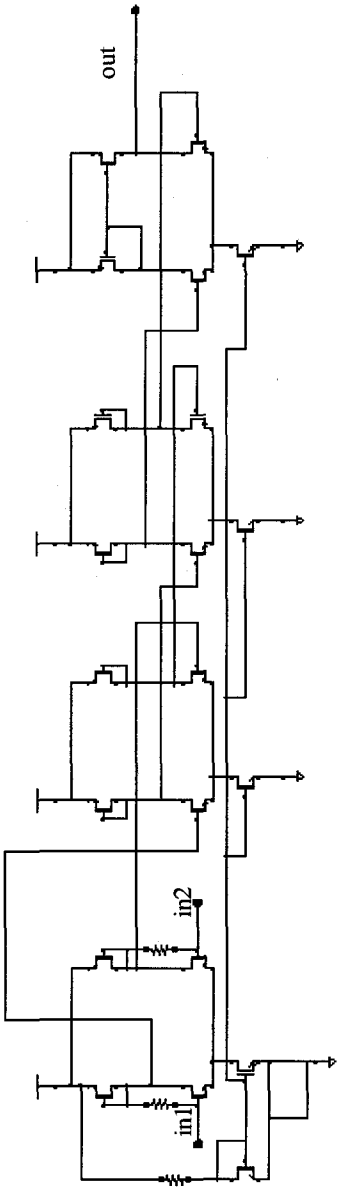

Figure 3.8 Front-end Amplifier

3.6 Layout Implementation

Figure 3.9 displays the layout of the chip. It has four circuits in the PAD ring. The upper left part is the front-end amplifier circuit. A zoom-in view is displayed in Figure 3.10. It should be noted that the layout of the two large transistors (width is 138 μm) uses multi-finger method in order to decrease the parasitic resistance. The bottom right part is the TIA circuit. A zoom-in view of this circuit is displayed in Figure 3.11. The upper right part is the first stage of the LA circuit and the bottom left part is the buffer stage of the LA. These two circuits are implemented to be used as testers in case that front-end amplifier fails.

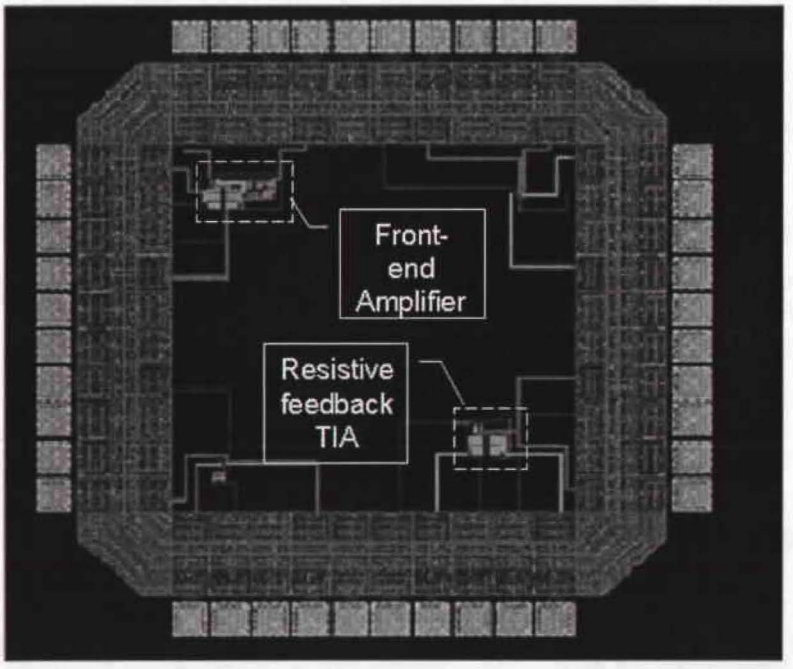

Figure 3.9 Whole Circuits Layout

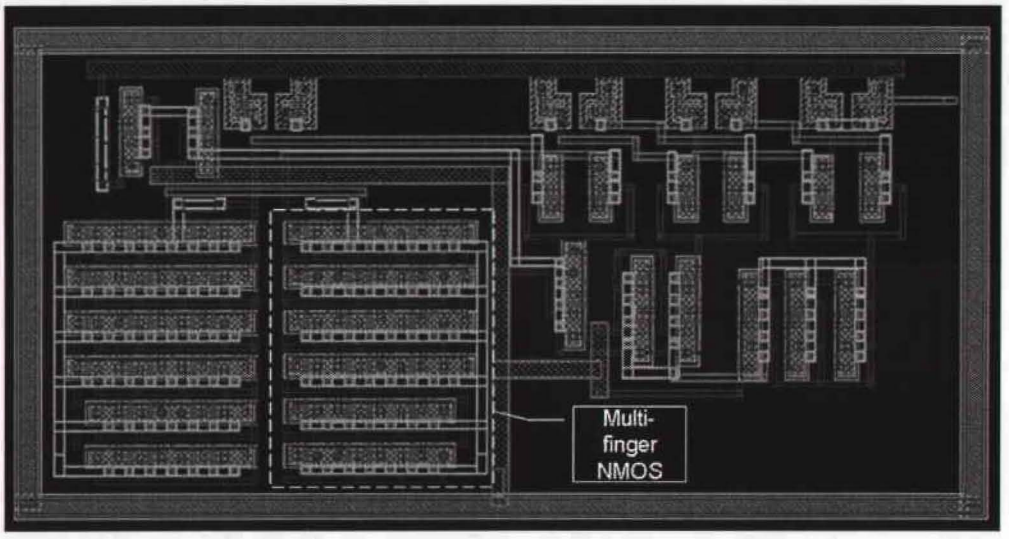

Figure 3.10 Front-end Amplifier Layout

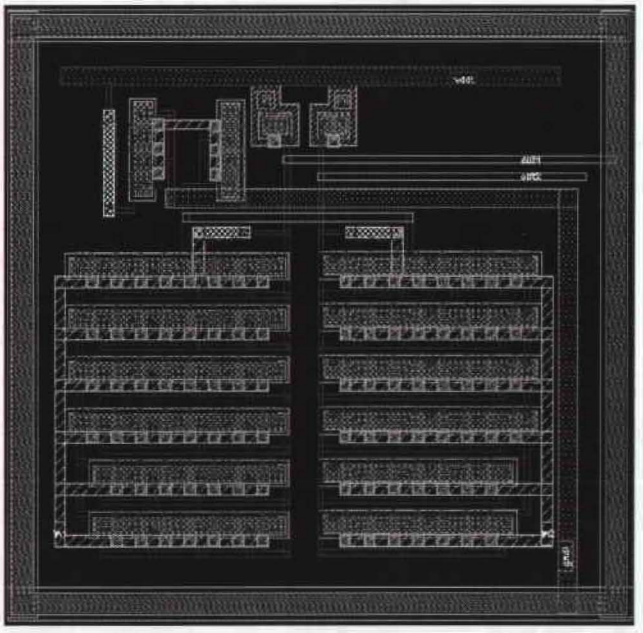

Figure 3.11 TIA Circuit Layout

Chapter 4. Simulation and Experiment Results

This Chapter presents the simulation results of the TIA, the LA and the front-end amplifier designed in the thesis project. The fabricated circuits were tested to corroborate the performance of the simulations.

4.1 Resistive Feedback TIA

The setup of the simulation of the TIA is shown in Figure 4.1. The two differential photodiode inputs to the TIA are modeled as two current sources of square wave. The current swings from 0μA to 20μA and the duty circle is 50%. Each of the sources is in parallel with a capacitor modeling the diode capacitance — a value of 0.5pF. The data, based on the simulation results, is summarized in the tables and figures below.

DC operation

in1(V)	in2(V)	out1(V)	out2(V)
2.323	2.323	2.368	2.368

Table 4.1 Simulated DC operation points of the resistive feedback TIA

Input and Output resistance

input resistance (K ohm)	5.179
output resistance (K ohm)	2.889

Table 4.2 Input and output resistance of TIA

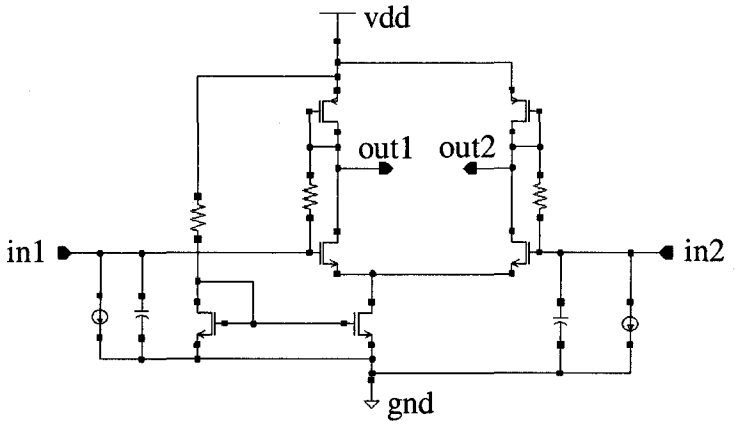

Figure 4.1 Simulation schematic of the TIA

Bandwidth

In order to perform the AC test, the two current sources of square wave are replaced by two current sources of sinusoid wave. Figure 4.2 and Figure 4.3 display the inputs and outputs at 10MHz respectively. As illustrated in Figure 4.4, the bandwidth of TIA is found to be 374.4MHz. Figure 4.5 shows that the TIA bandwidth can be increased if the input capacitance mainly resulting from the photo-diode is decreased.

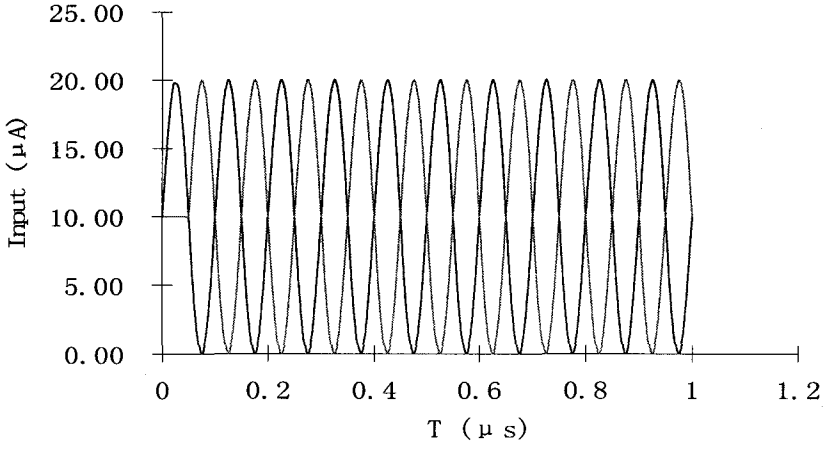

Figure 4.2 Differential sinusoid inputs of the TIA at 10MHz

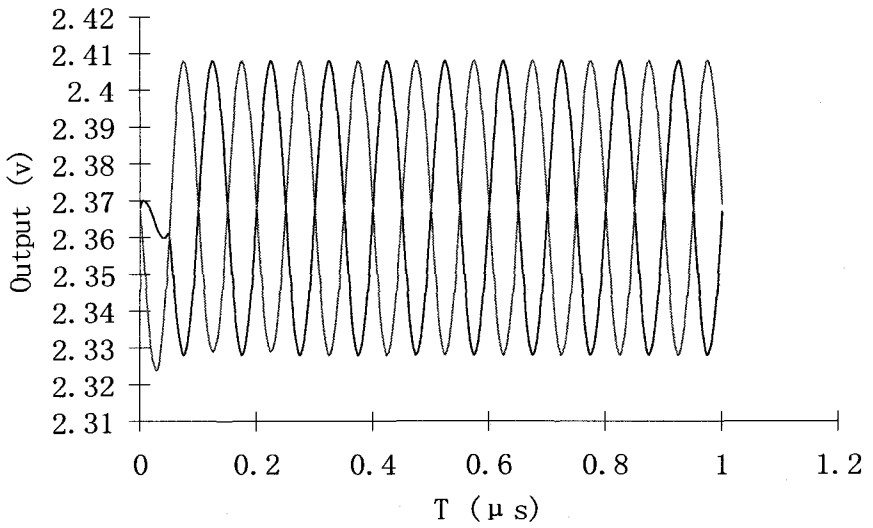

Figure 4.3 Differential sinusoid outputs of the TIA at 10MHz

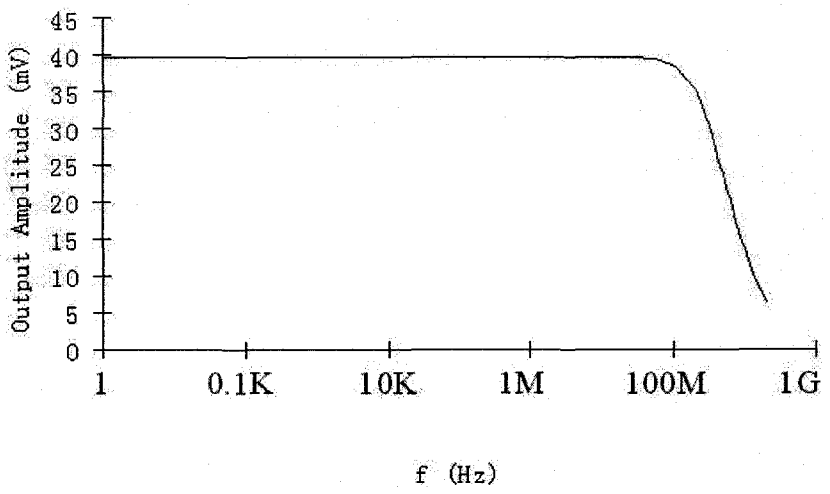

Figure 4.4 Output amplitude vs. frequency

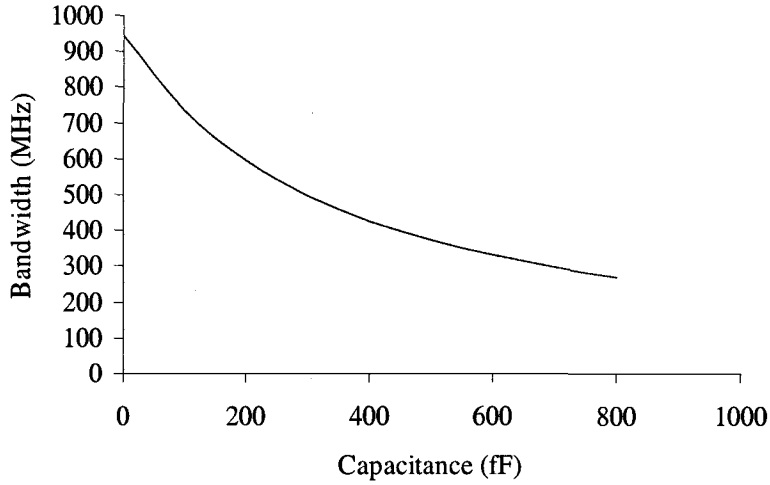

Figure 4.5 The bandwidth of TIA vs. input diode capactiance

Output Response and Transimpedance Gain

The output AC response of the TIA to the square wave inputs is studied at different frequencies. An example of the differential inputs at 1KHz is shown in Figure 4.6. The output responses at different frequencies are illustrated from Figure 4.7 to Figure 4.10. When the frequency is below the bandwidth, the outputs keep square wave response and the swing is 80mV. Thus the transimpedance gain is given by

$$\frac{V_{out}}{I_{in}} = \frac{80mV}{20\mu A} = 4k\Omega \tag{4.1}$$

When the frequency increases beyond the bandwidth, the waveform of the outputs deviates from desired waveform. The reason is that the settling time is not small enough with respect to the period of the input.

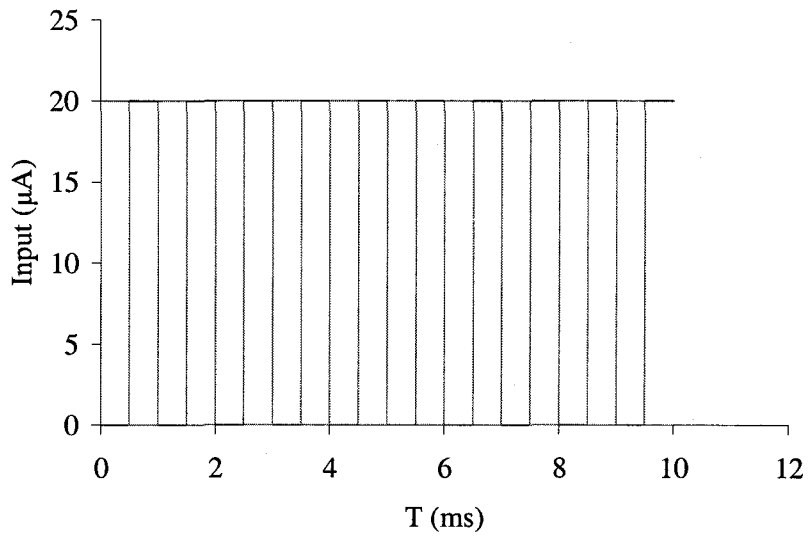

Figure 4.6 Differential inputs of square wave at 1KHz

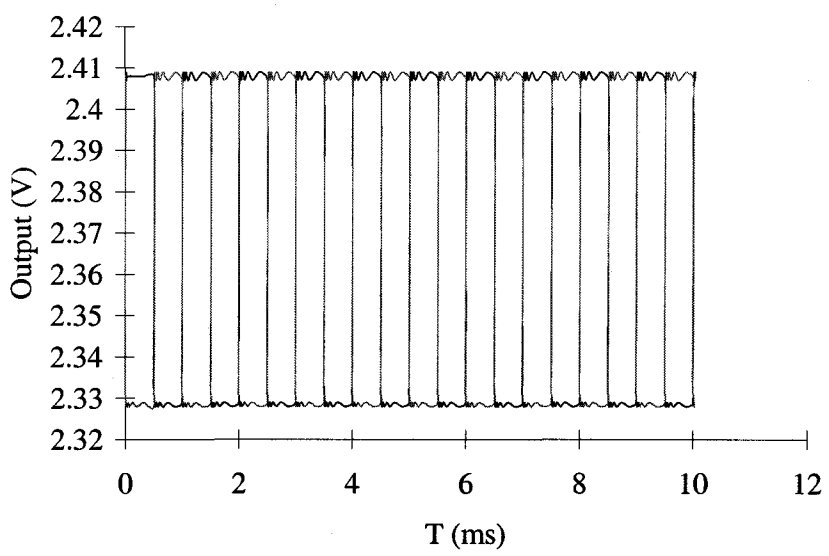

Figure 4.7 Output response of the TIA at 1KHz

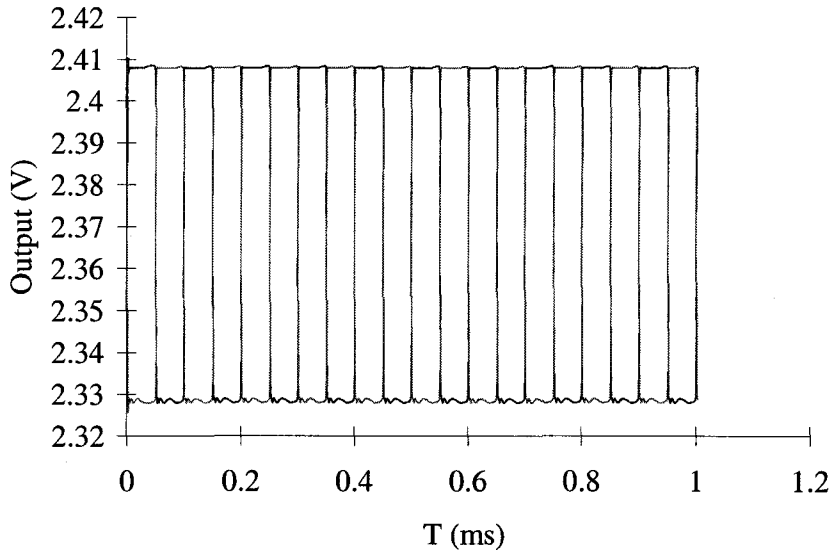

Figure 4.8 Output response of the TIA at 10KHz

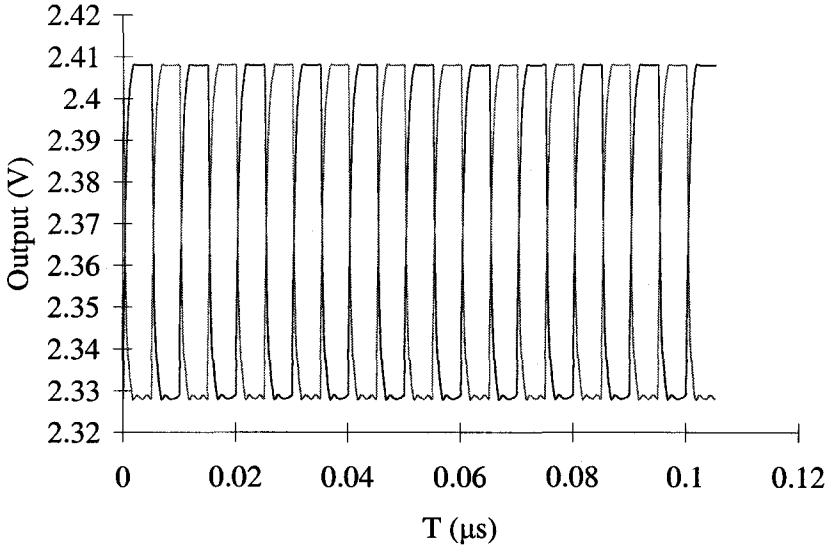

Figure 4.9 Output response of the TIA at 100MHz

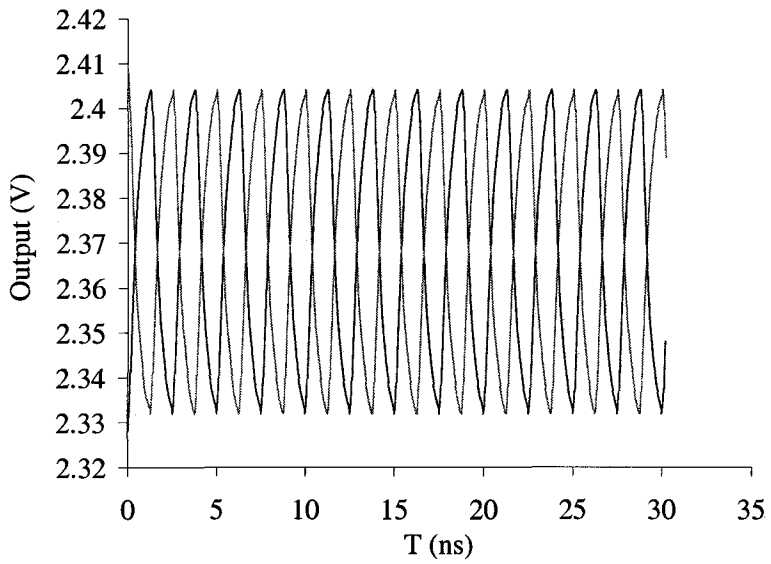

Figure 4.10 Output response of the TIA at 400MHz

The fabricated TIA circuit is tested in order to verify the simulation results. Figure 4.11 illustrates the experiment setup. Two differential voltage signals are generated by the pulse wave generator as shown in Figure 4.12. The voltage swing is 4.02V. The duty cycle is 50%. The signals are fed into the nodes of input1 and input2. Each of them is placed in series with a resistor in order to create a current source. The resistor value is $196k\Omega$, in order to create a current swing of $20\mu A$:

$$I_{swing} = \frac{V_{swing}}{R+R_{in}} = \frac{4.02V}{196k\Omega+5.2k\Omega} \approx 20\mu A \tag{4.1}$$

where R_{in} is the input impedance of the circuit. From the simulation results, we know the input resistances of the resistive feedback TIA to be around $5.2k\Omega$. Therefore the inputs to the node of in1 and in2 of the TIA can be viewed as square wave current sources, which swing from $0\mu A$ to $20\mu A$.

The output signals of the TIA, from the node of out1 and out2, are filtered by a capacitor in order to eliminate the high frequency noise. The filtered signals are sensed by oscilloscope probes at the nodes of output1 and output2. The power supply probe and the ground probe are used to provide a supply voltage of 5 volts and common ground to the TIA circuit respectively. The breadboard is used for resistors, capacitors and common ground connections. The measured experiment results are shown in the table and figures below.

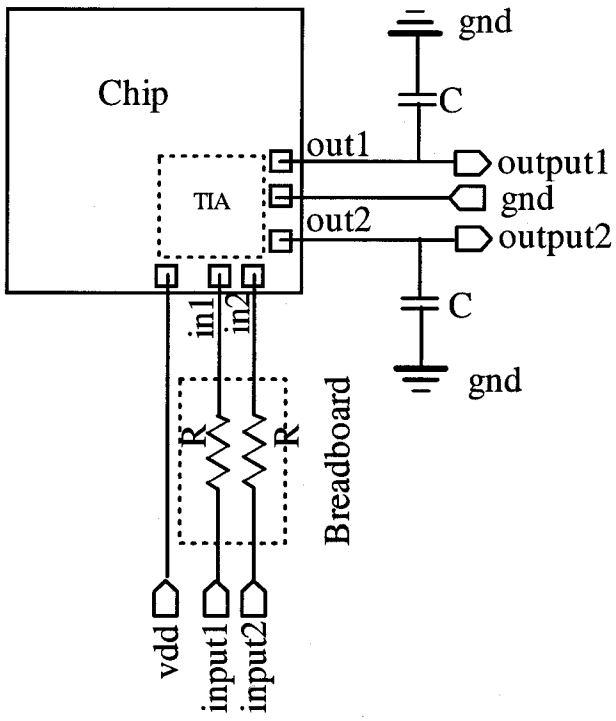

Figure 4.11 Resistive feedback TIA test setup

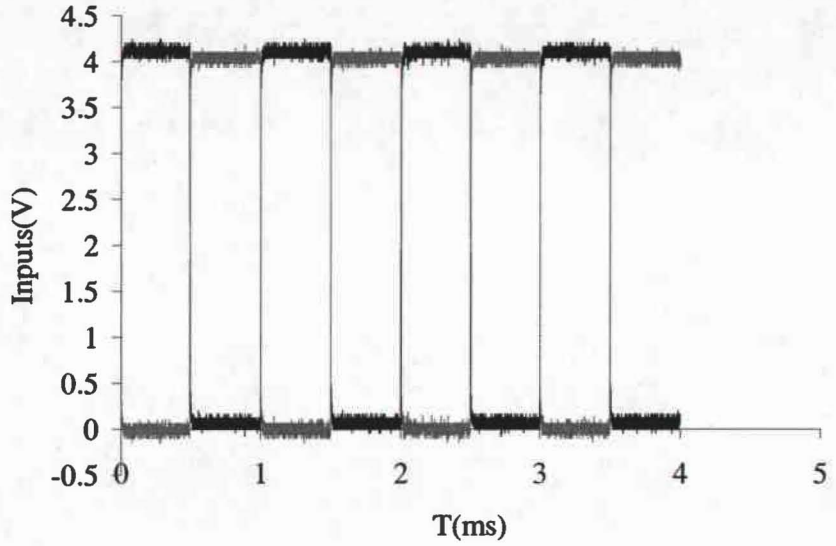

Figure 4.12 Differential signals generated by the pulse wave generator

DC operation

The DC operation points of the experimental measurement are very close to those of the simulation results. To evaluate, the relative error is given by

$$\text{Relative Error} = \left| \frac{\text{Real Test Value} - \text{Simulation Value}}{\text{Simulation Value}} \right| \times 100\% \tag{4.2}$$

All the relative errors mentioned later are calculated according to this equation. From the data in Table 4.3, we notice that the relative error to be less than 0.8%. It indicates that the TIA circuit works in the proper DC operation point in the experiment.

Nodes	in1	in2	out1	out2
Simulation	2.323V	2.323V	2.368V	2.368V
Real Test	2.313V	2.316V	2.352V	2.355V
Relative Error	0.4%	0.3%	0.7%	0.5%

Table 4.3 Simulated and tested DC operation points of resistive feedback TIA

Output Response at Low Frequency and Transimpedance Gain

The AC output response of the TIA is tested at 1KHz and 10KHz, with the DC level shifted to zero volt. The results are illustrated in Figure 4.13 and Figure 4.14. There is a considerable amount of noise observed at the output nodes. We attribute this noise to the experimental setup because the noise from the DC supply cannot be decoupled when using DC probe. The output swing is approximately 70mV, whereas the simulation suggested this value to be 80mV. Therefore, based on the experimental data, the transimpedance gain is found to be $3.5k\Omega$. As mentioned earlier, the AC measurement was carried out only at low frequencies – use of DC probe and large parasitic capacitances and inductances limit the measurement frequency.

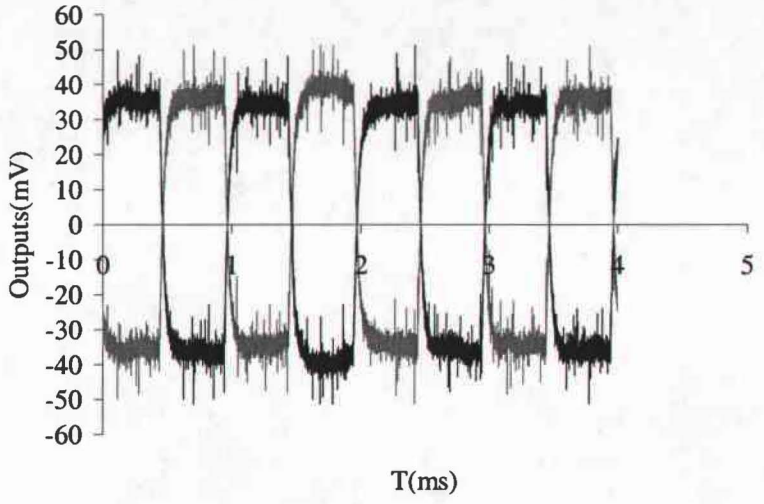

Figure 4.13 Outputs of the TIA at 1KHz

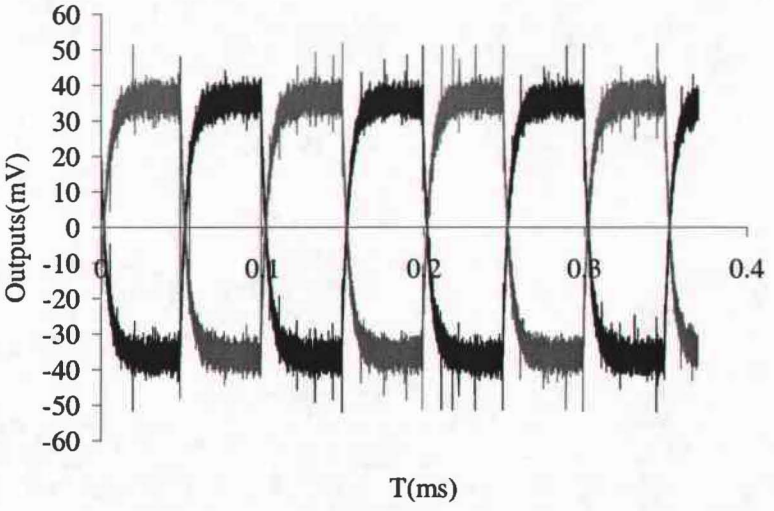

Figure 4.14 Outputs of the TIA at 10KHz

In order to improve the noise and bandwidth limitations caused by the measurement set up, a PCB board was fabricated to test the packaged chip. Both the TIA and the front-end amplifier were tested using an oscilloscope, model Agilent 54832D and probes,

model Agilent 1144A. The PCB layout and the schematic are shown in Figure 4.15 and Figure 4.16, respectively. Two decoupling capacitors were used on the PCB - one with value of 47μF was placed near the DC supply and the other with value of 0.1μF was placed near Vdd of the chip.

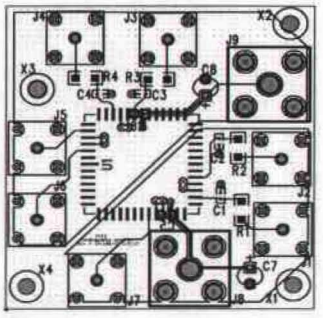

Figure 4.15 The layout of PCB testboard

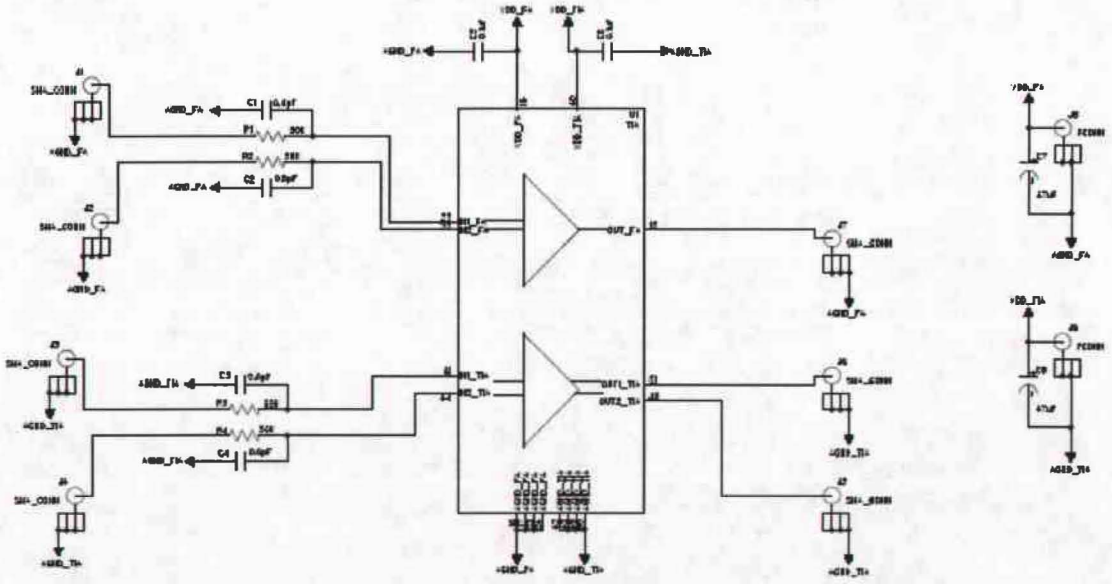

Figure 4.16 The schematic of PCB testboard

Bandwidth

The experimental and simulation results of TIA at different frequencies are shown in Figure 4.17. The cutoff frequency of the amplifier is measured to be 27MHz. This is considerably less than what was anticipated and was due to the low output impedance of the amplifier and the loading effect of the probe. Because the TIA output resistance is around 2.9 Kohm and the probe capacitance is 2pF, the output amplitude is limited by the low output impedance at higher frequencies. Simulation of the TIA circuit with probe capacitance as a load results in a bandwidth of 26 MHz, which is close to the value of the bandwidth (24 MHz) measured.

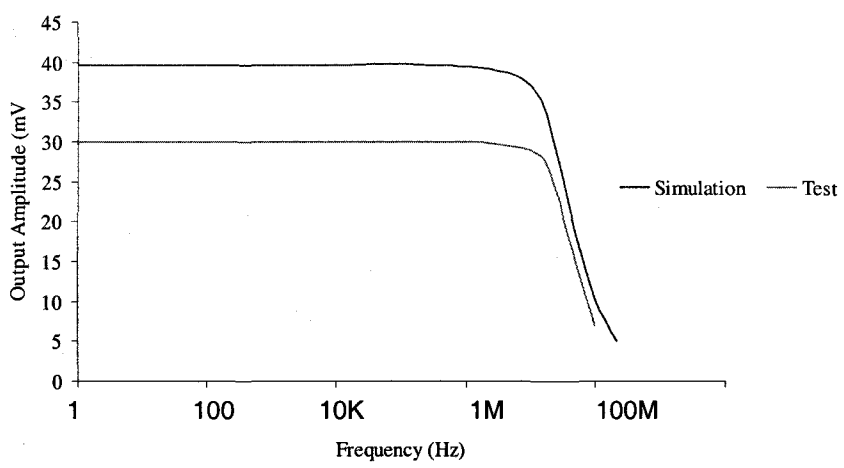

Figure 4.17 The output amplitude of TIA vs. frequency

Output Response at High Frequency and Transimpedance Gain

As shown in Figure 4.18 and Figure 4.19, the output noise is greatly reduced. The noise amplitude using the PCB is around 5mV, whereas this value is more than 10mV in

the set up that involved using the breadboard. The output swing of the PCB test is 60mV. Therefore, the transimpedance gain is 3kΩ. The response to the square wave input will not distort until the frequency exceeds the bandwidth.

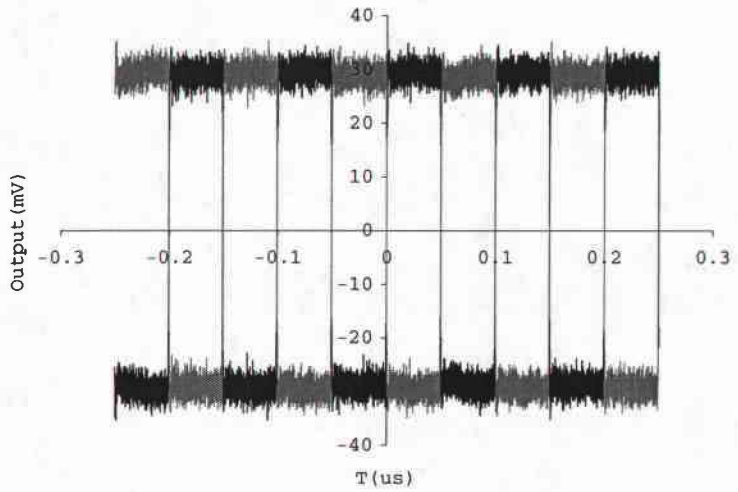

Figure 4.18 Outputs of TIA at 10MHz

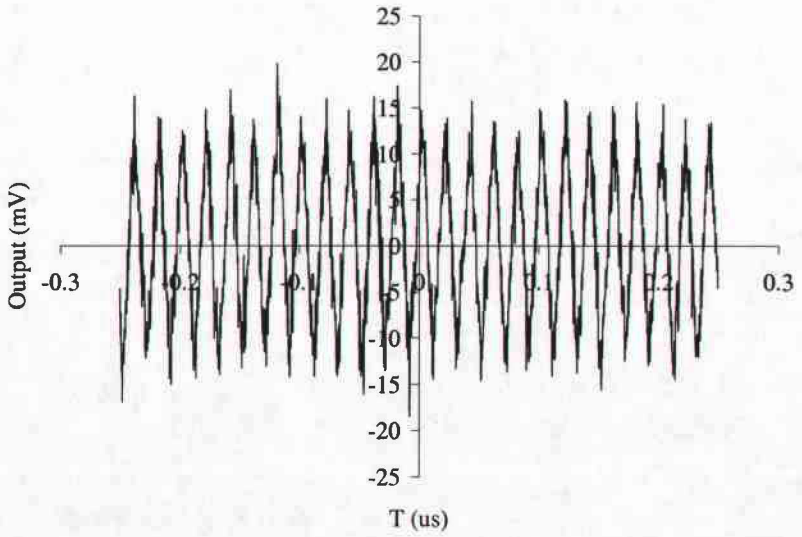

Figure 4.19 One output of TIA at 50MHz

4.2 Limiter Amplifier

The simulation schematic is shown in Figure 4.20. Two voltage sources are applied at the two inputs nodes. They are biased at the DC level of 2.368V. This value is set according to the DC level of outputs the TIA. The simulation results are illustrated in the tables and figures below.

DC operation

In1 (V)	In2 (V)	Out (V)
2.368	2.368	2.377

Table 4.4 DC operation points of LA

Input and Output Resistance

The input resistance of LA is 1T ohm, which is equal to 10^{12} ohm. It is very large because the gate resistor of MOS is a very large.

Input Resistance (T ohm)	1
Output Resistance(K ohm)	107.1

Table 4.5 Input and Output Resistance of LA

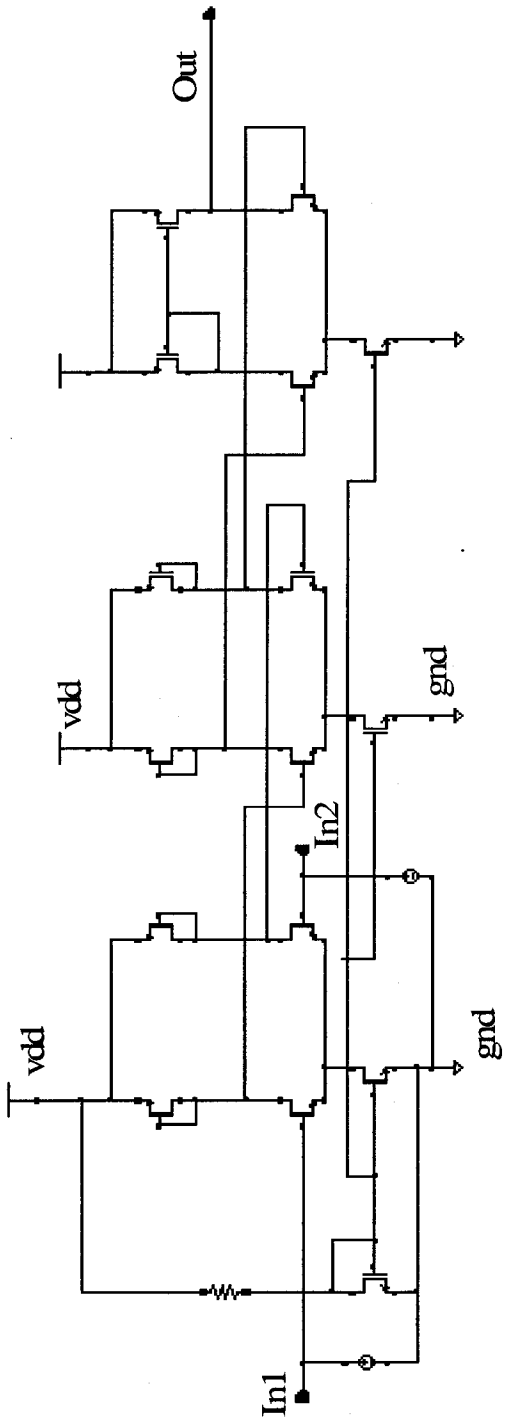

Figure 4.20 The simulation schematic of the LA circuit

Input Voltage vs. Output Voltage

As shown in Figure 4.21, when the input swing exceeds 10mV, the output is non-linear. It is because the second and the third stages of the LA operate in the saturation region. This characteristic is expected in the LA circuit design and can be used as an effective way to regulate the output signal of TIA. When TIA output is no longer a perfect square waveform, the LA is able to regulate the input signal to be acceptable square waveform. This regulation characteristic is further studied in the output response of the limiter amplifier.

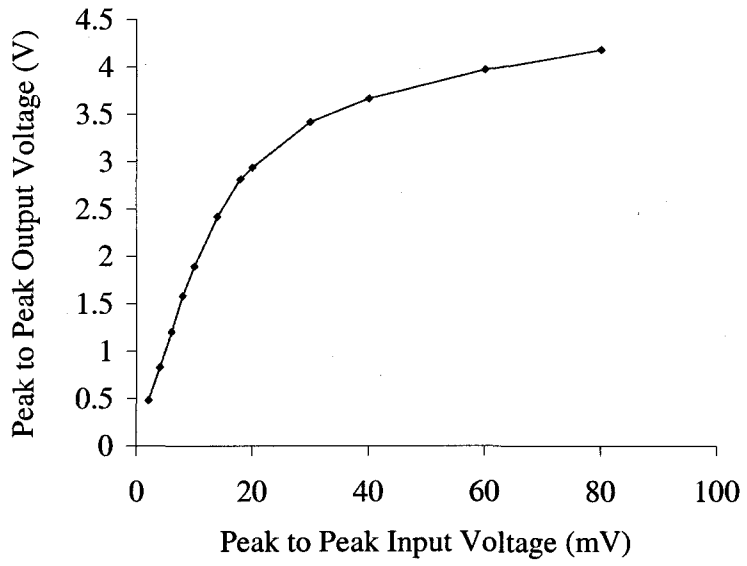

Figure 4.21 The input voltage swing vs. output voltage swing of LA

Bandwidth

In order to ensure the LA linear operation, the input swing is set to be as small as 6mV. Thus the output at different frequency can be plotted as shown in Figure 4.22. The bandwidth estimated from simulation of the LA is 586.8MHz.

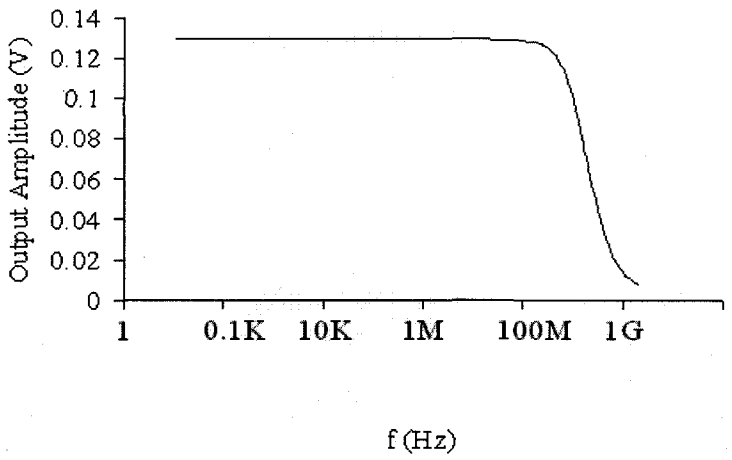

Figure 4.22 Voltage gain vs. Bandwidth

Output Response and Output Swing

The output AC response of the LA is studied in two extreme cases. One case is when the input signal is an ideal square wave as shown in Figure 4.23. The input swing is 80mV. The outputs are also square wave as shown in Figure 4.24, with a voltage swing of 4.2V.

The other case is when the input signal is 80mV triangular wave as shown in Figure 4.25. Figure 4.26 shows that the output waveform has the resemblance of a square wave with an output swing of 4.2V. Therefore, even when the output of the TIA may somewhat deviate from the desired waveform due to limitations in its design, the output of the LA is not severely impacted.

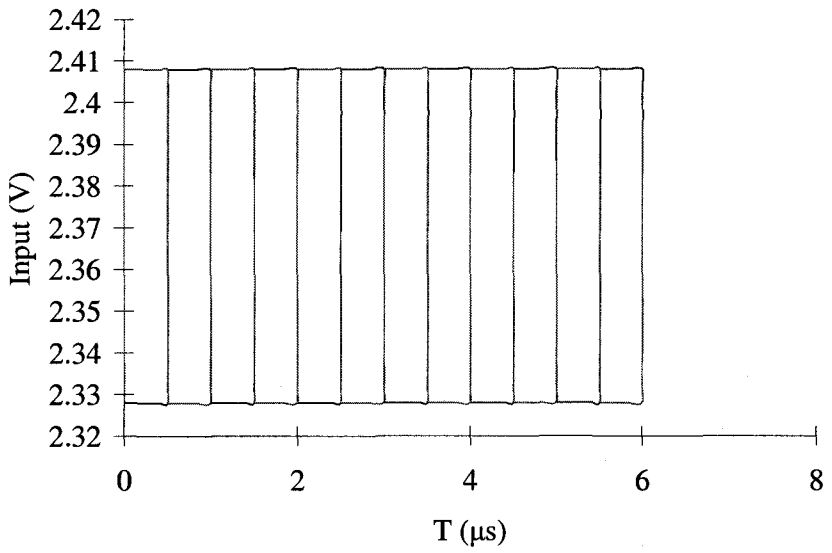

Figure 4.23 The square wave inputs of LA at 1MHz

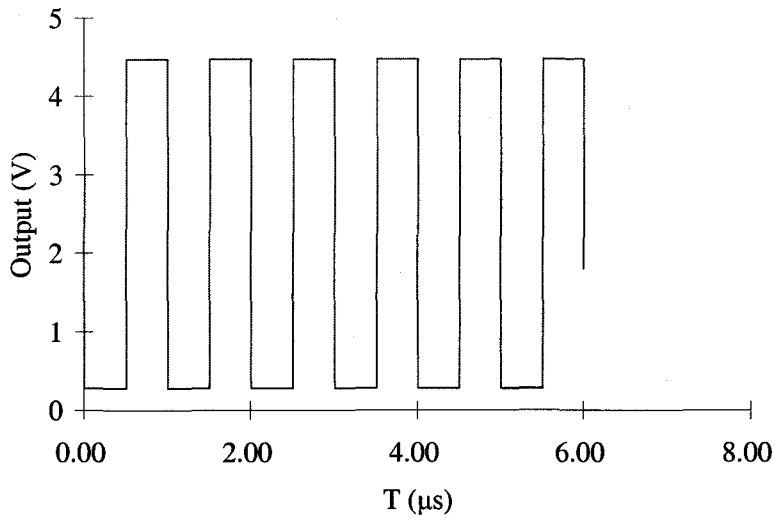

Figure 4.24 The square wave outputs of LA at 1MHz

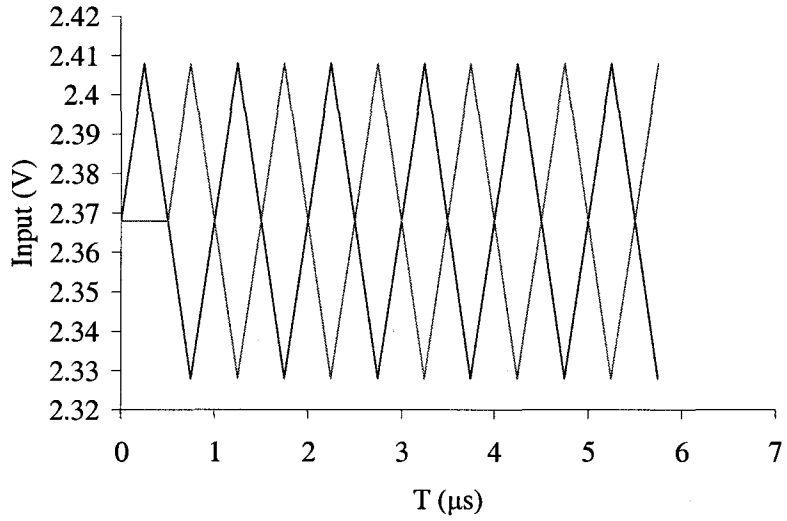

Figure 4.25 The inputs of triangle waveform of the LA at 1MHz

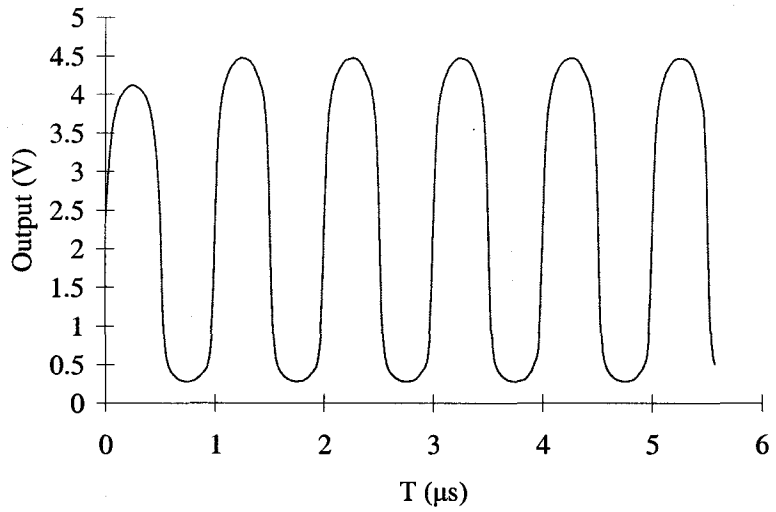

Figure 4.26 The outputs of LA at 1MHz

4.3 Front-end Amplifier

The simulation schematic of the front-end amplifier is shown in Figure 4.27. The setup is as the same as that of the TIA. The simulation results are illustrated in the tables and figures below.

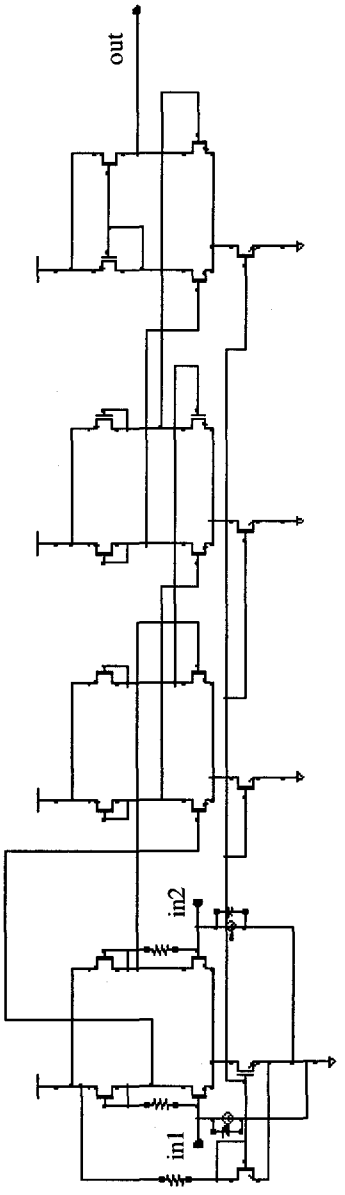

Figure 4.27 Simulation schematic of the front-end amplifier

DC operation

in1 (V)	in2 (V)	out (V)
2.168	2.168	2.261

Table 4.6 Simulated Front-end Amplifier Operation Point

Input and Output Resistance

Input Resistance (K ohm)	5.196
Output Resistance (K ohm)	49.02

Table 4.7 Input and out resistance of front-end amplifier

Output Response and Output Swing

The output AC response of the front-end amplifier is studied at different frequencies, as shown from Figure 4.28 to Figure 4.31. The output swing is 4.2V. It can be observed that the waveform of the outputs keeps square wave when the frequency is below the bandwidth of the TIA. When the frequency exceeds the bandwidth, the output waveform exhibits distortion.

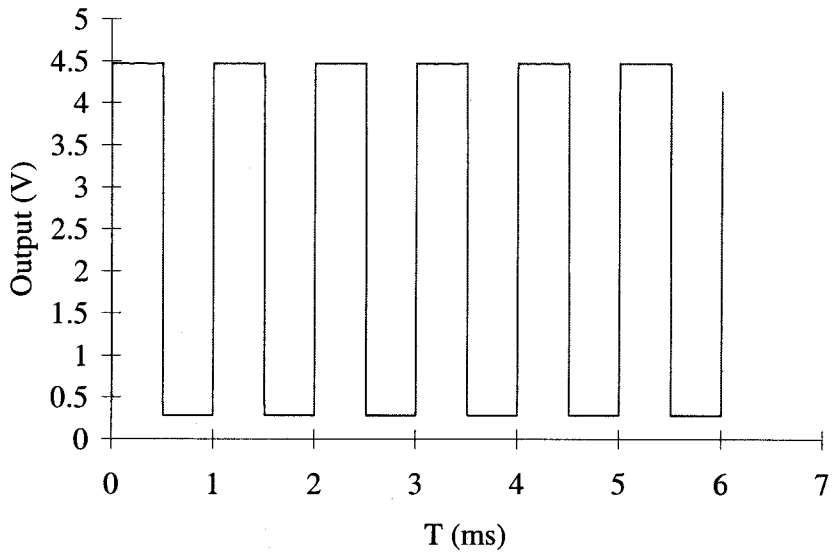

Figure 4.28 Output response of front-end amplifier at 1KHz

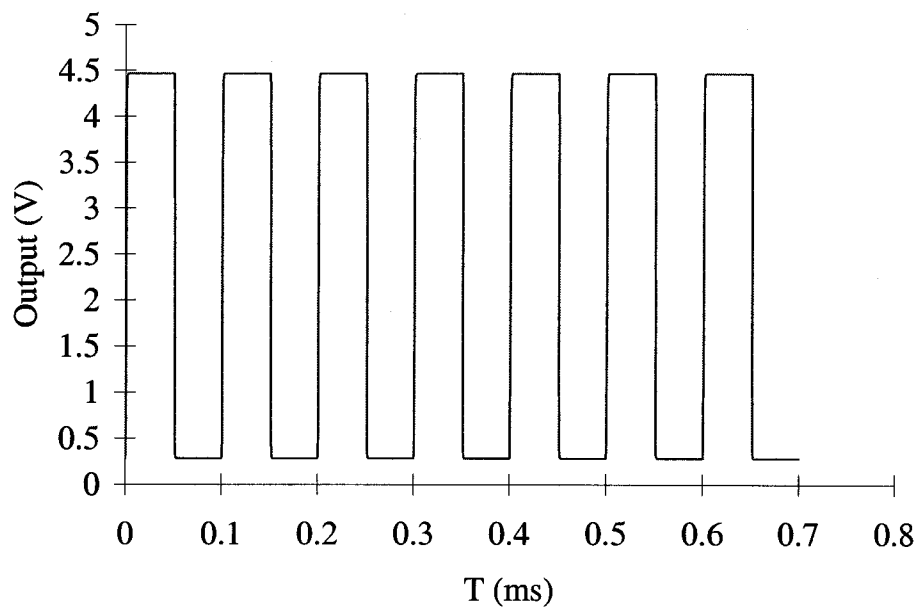

Figure 4.29 Output response of front-end amplifier at 10KHz

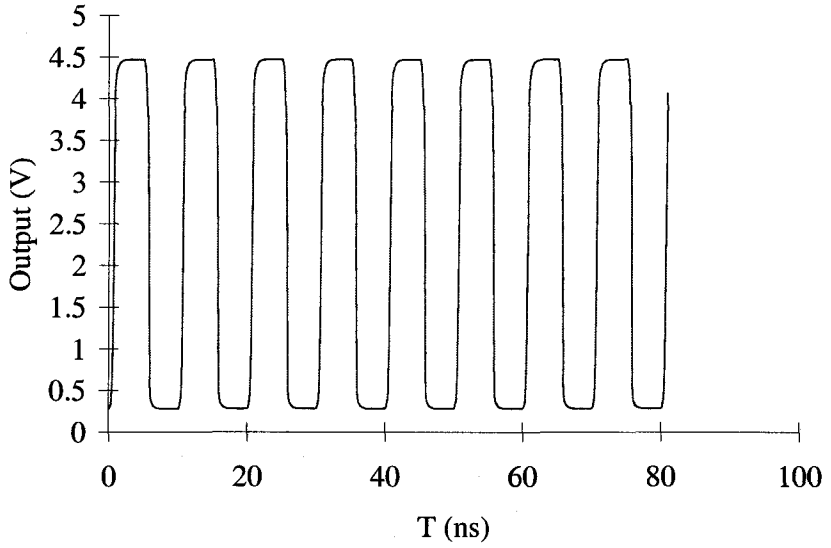

Figure 4.30 Output response of front-end amplifier at 100MHz

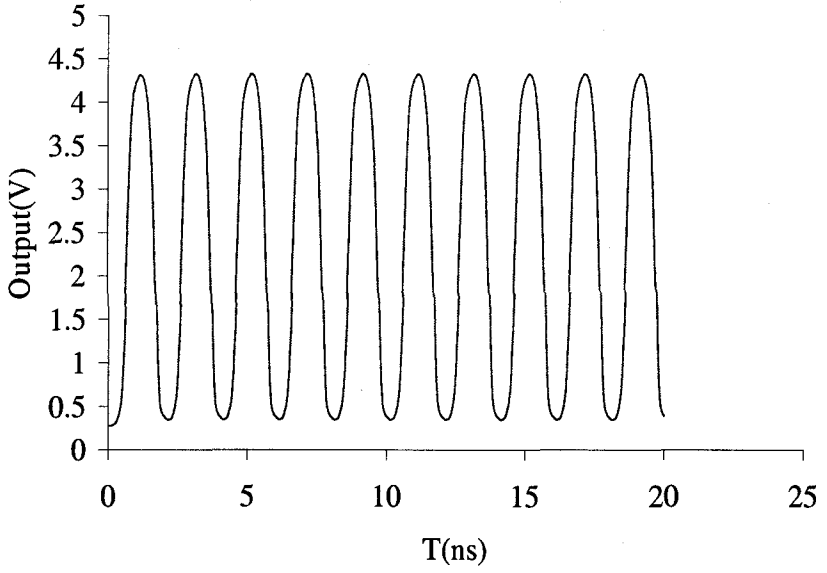

Figure 4.31 Output response of front-end amplifier at 500MHz

In order to verify the simulation results, the fabricated front-end amplifier circuit is tested. The Figure 4.32 illustrates the experiment setup which is similar to the setup for the TIA test as described above. The only difference is the output does not have a filter capacitor. Because the front-end amplifier and the TIA have the same input resistance value, the current inputs to the front-end amplifier are also square waves which swing from $0\mu A$ to $20\mu A$. The experiment results are shown in the tables and figures below.

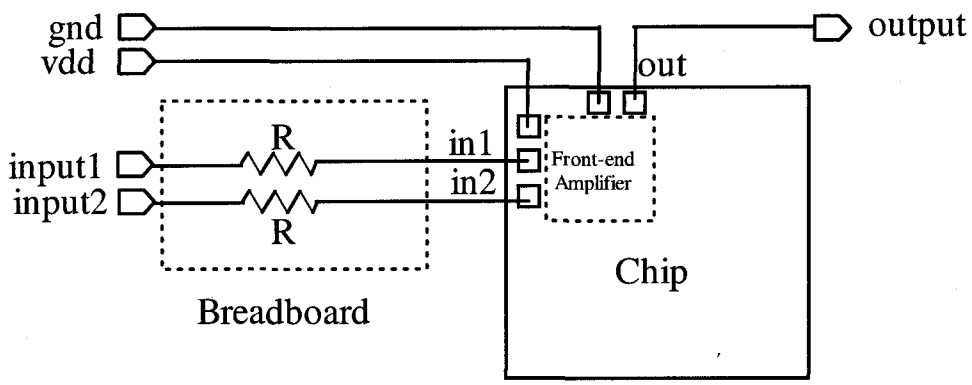

Figure 4.32 Front-end amplifier test setup

DC operation

Table 4.8 displays the data of the DC operation points of the front-end amplifier. The real test results are close to those of the simulation results because the absolute value of the relative error is not larger than 3%. It indicates that the front-end amplifier works at proper operation points.

	in1	in2	out
Simulation	2.168V	2.168V	2.261V
Real Test	2.235V	2.230V	2.33V
Relative Error	3%	3%	3%

Table 4.8 Simulated and tested DC operation points of front-end amplifier

Low Frequency Output Response

Figure 4.33 shows the test results of output response of front-end amplifier. The output swing is approximately 4.1V. The relative error is 2%.

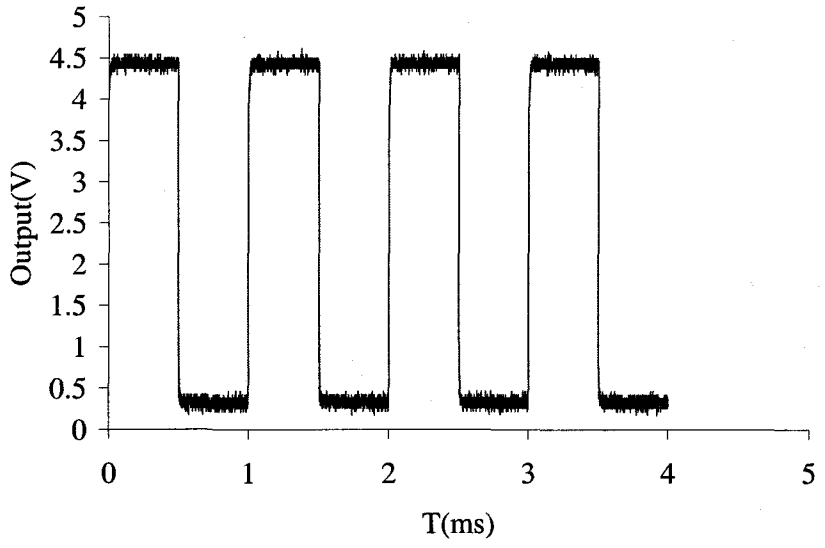

Figure 4.33 Output of front-end amplifier at 1KHz frequency

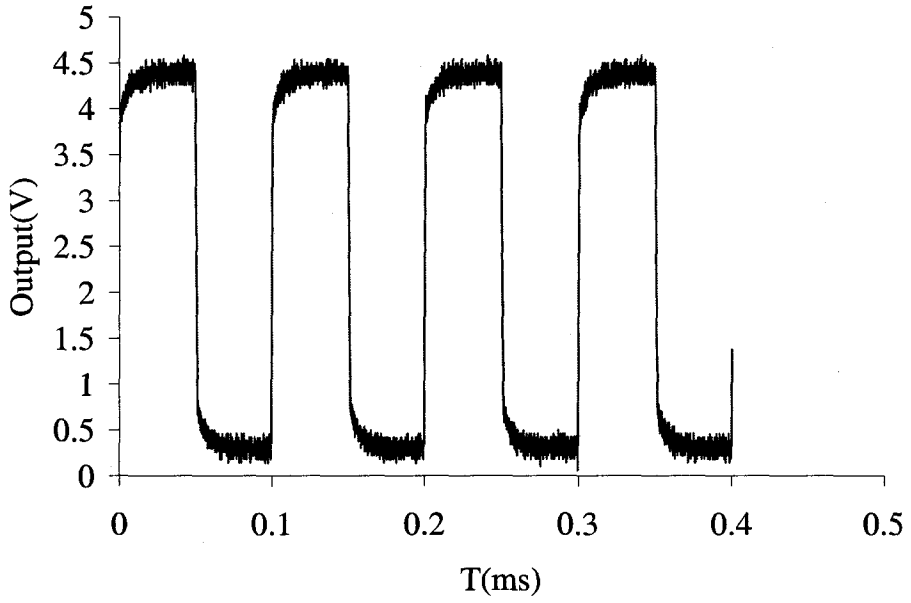

Figure 4.34 Output of the front-end amplifier at 10KHz frequency

As previously mentioned, the PCB board test is performed to test the high frequency performance of the front-end amplifier. Similar to the results of TIA discussed earlier, the measured bandwidth is lower than anticipated because of the loading effect of probe capacitance. As illustrated in Figure 4.35, experimental measurement and simulation, which include the probe capacitance as the load, lead to bandwidth values of 1.6 MHz and 1.5 MHz, respectively. Figure 4.36 and Figure 4.37 show the output response to square wave inputs at two different frequencies.

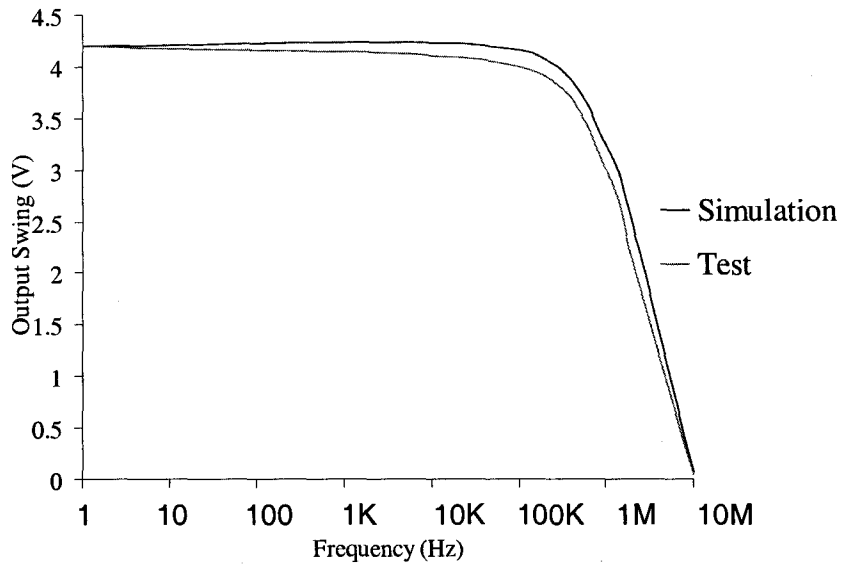

Figure 4.35 Output swing of front-end amplifier vs. frequency

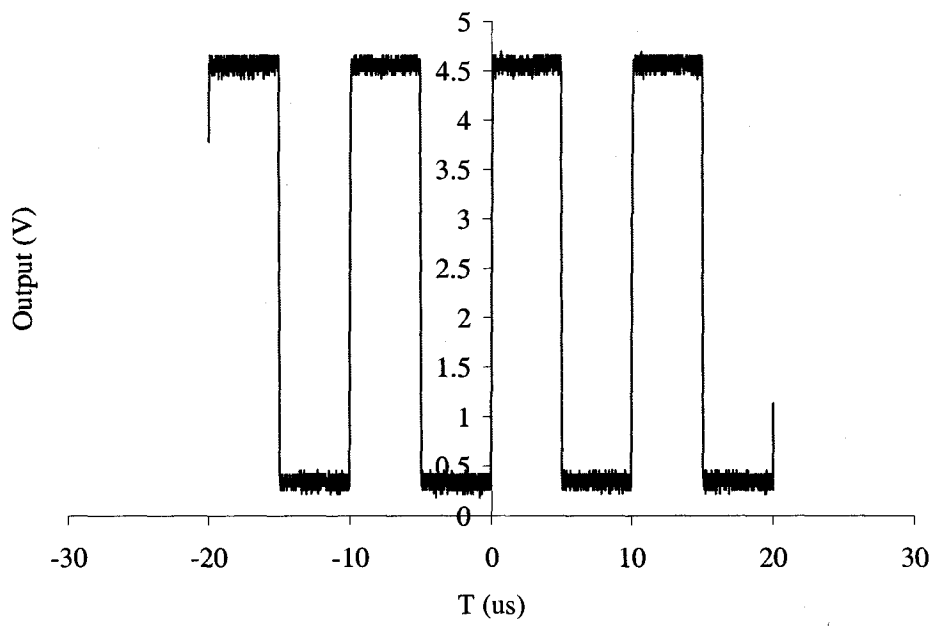

Figure 4.36 Outputs of front-end amplifier at 100KHz

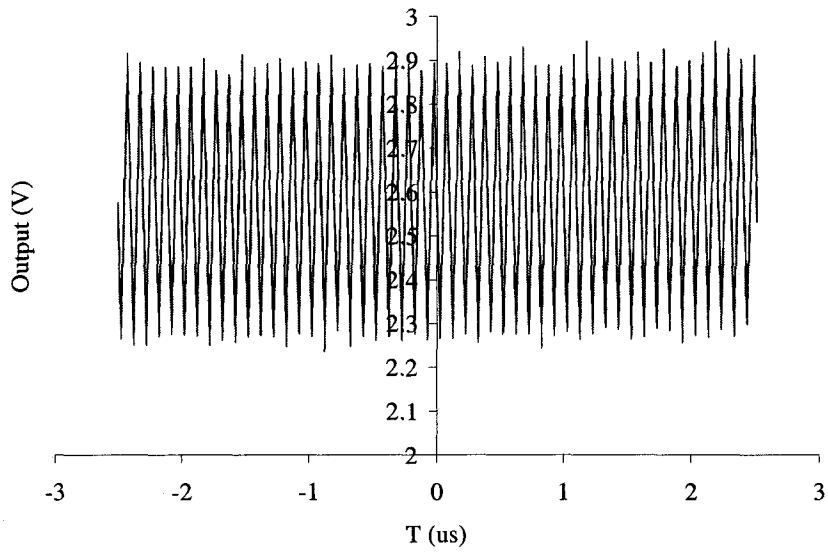

Figure 4.37 Outputs of front-end amplifier at 1MHz

4.4 Inductive Peaking

The simulation setup for series inductive peaking is shown as Figure 4.38. The sources are the same as the ones used for the resistive feedback TIA. While changing the inductance value, the bandwidth is estimated and the result is illustrated in Figure 4.39. When the inductance approaches 10μH, the bandwidth is increased to 600MHz. However, this is not a practical approach because the inductance value is too large for on chip design.

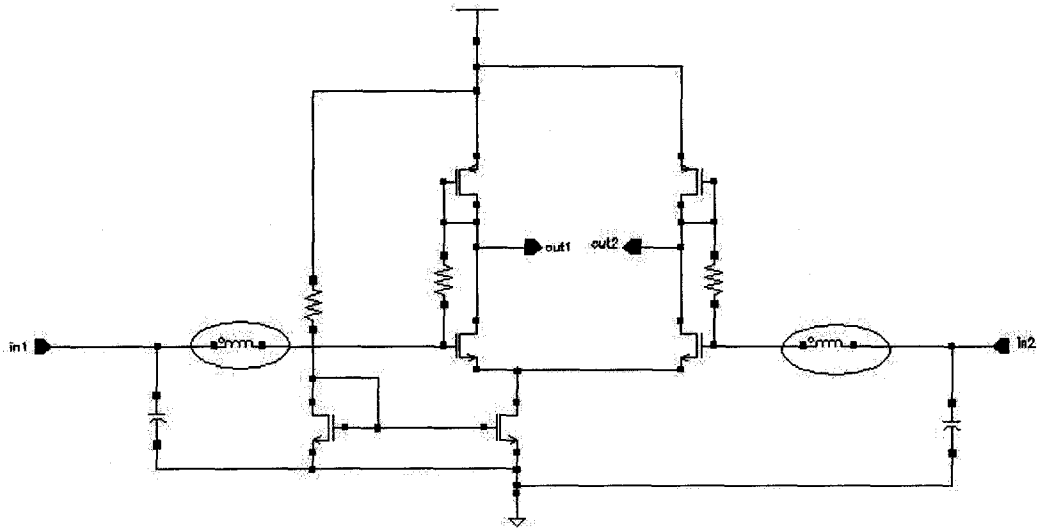

Figure 4.38 Simulation schematic for series inductive peaking

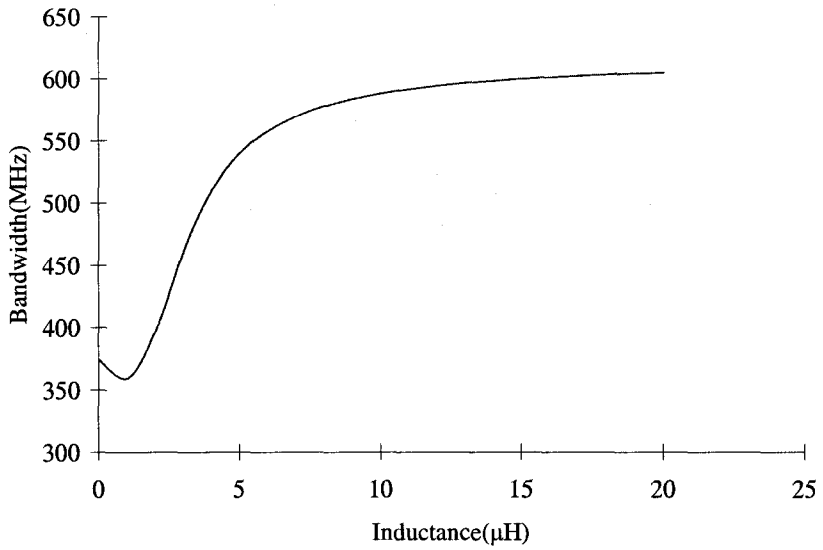

Figure 4.39 Bandwidth enhancement vs. inductance by series inductive peaking

The same measurement on the series inductive peaking is performed. The simulation schematic is displayed as Figure 4.40. As shown in Figure 4.41, the bandwidth is 440MHz when the inductance reaches 20nH. Therefore, the shunt inductive peaking can be considered as an approach for future research for the TIA.

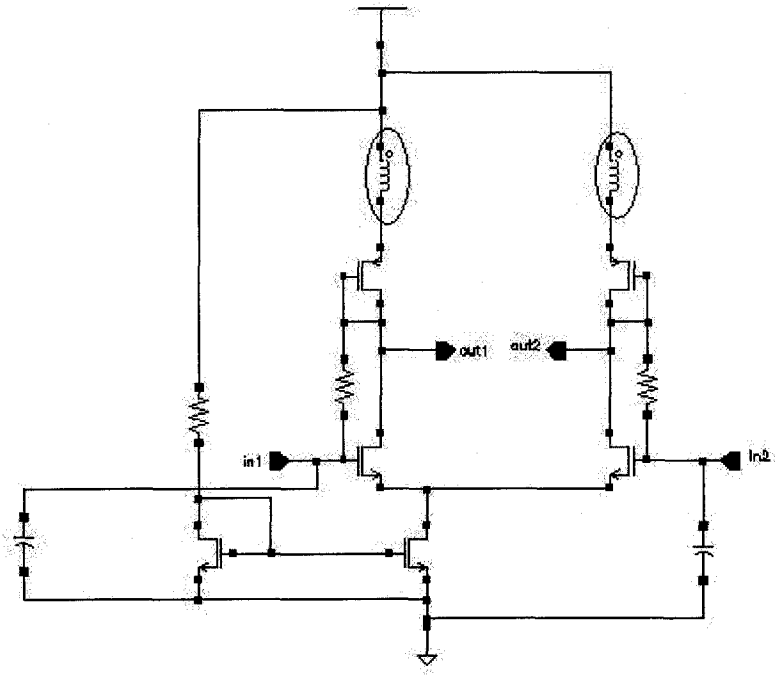

Figure 4.40 Simulation schematic of shunt inductive peaking

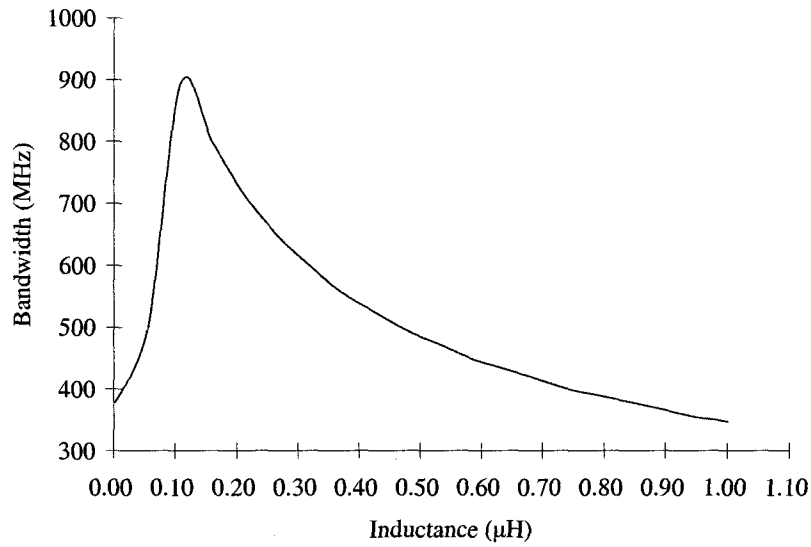

Figure 4.41 Bandwidth enhancement vs. inductance by shunt inductive peaking

4.5 Summary

A summary of results is presented in Table 4.9. Whenever possible, the results from simulation are validated through experimental measurements. Due to limitations in the experimental setup, AC measurements have been limited to low frequencies. The bandwidth parameter cannot be verified in the experiment. Inductive peaking is justified at the simulation level. The benefits of inductive peaking are explored at the simulation level. The shunt inductive peaking can be considered as an approach for future research for the resistive feedback TIA circuit design, with significant potential enhancement in the circuit's bandwidth.

Parameter	*Proposed Value*	*Simulation Results*	*Experiment Results*
Data Rate	500Mb/s	535Mb/s	N/A
TIA Bandwidth	350MHz	374.4MHz	N/A
TIA Gain	3 kΩ	4 kΩ	3 kΩ
LA Bandwidth	450MHz	586.8MHz	N/A
LA Output Swing	3.5V	4.2V	4.1V
Diode Light Current	20 μA	20 μA	20 μA
Diode Capacitance	0.5pF	0.5pF	0.5pF

Table 4.9 The summary of the proposed values, simulation and experiment results

Chapter 5. Summary and Conclusion

The front-end amplifier, composed of a TIA and a LA, plays an important role in the fiber optical system. The data rate of the optical system is largely determined by the bandwidth, the transimpedance gain and the noise of the TIA. The LA circuit must boost the output of the TIA to at least 250mV to drive the DMUX stage for data recovery.

In this thesis project, simulations for the TIA, the LA and the complete front-end amplifier are conducted in the Cadence design environment cooperated with the NCSU design kit. The TIA and the front-end amplifier is fabricated using the AMI 0.5 μm CMOS process. The test is performed using a probe station and breadboard to verify the design.

Three design topologies including common-gate TIA, resistive feedback TIA and capacitive feedback TIA are examined. The resistive feedback TIA is selected for the thesis project design for two reasons. First, the resistive feedback TIA generates the smallest noise among the three topologies. Second, the realization of the resistive feedback TIA avoids using any on-chip capacitor or inductor, which the AMI 0.5 μm CMOS process does not supply. The simulation results reveal that the estimated bandwidth of the TIA is 374.4MHz and the transimpedance gain is 4 kΩ . The experimental determined transimpedance gain is 3 kΩ .

The topology used to design the LA circuit is cascaded gain stages. There are three gain stages used. The first two stages are the differential resistive load amplifiers. The last stage is a buffer to convert the differential outputs to a single-end output. The

simulation results show that the bandwidth of the LA is 586.8MHz and the output swing is 4.2V.

The complete front-end amplifier is implemented by cascading the TIA and the LA together. According to the simulation data, the front-end amplifier achieves a data rate of 535Mb/s. The simulated output swing is 4.2V, while the experimental output swing measured is found to be s 4.1V. Due to the constraints of the probe load effect, the functionality of the two circuits is demonstrated up to 20MHz. Designing a buffer at the end of the TIA and the front-end amplifier to transfer the impedance to 50 ohm may enable the test to go up to GHz frequency range.

The technique of inductive peaking for enhancing the bandwidth of a TIA is also explored through simulation. The simulation results reveal that the shunt inductive peaking may help increase the bandwidth of the circuit and may be considered for future development of CMOS-based TIA design.

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2 A.K. Petersen, K. Kiziloglu, T. Yoon, F. Williams, and M.R. Sandor, "Front-end CMOS Chipset for 10 Gb/s Communication", *IEEE Radio Frequency Integrated Circuits Symposium*, June 2002, pp. 93-96.

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